IN THE UNITED STATES DISTRICT COURT
FOR THE SOUTHERN DISTRICT OF FLORIDA

TURBOCODE LLC,

Plaintiff,

v.

AIRSPAN NETWORKS INC.,

Defendant.

C.A. No. ______________

JURY TRIAL DEMANDED

PATENT CASE

ORIGINAL COMPLAINT FOR PATENT INFRINGEMENT

Plaintiff TurboCode LLC files this Original Complaint for Patent Infringement against Airspan Networks Inc., and would respectfully show the Court as follows:

I. THE PARTIES

1. Plaintiff TurboCode LLC ("TurboCode" or "Plaintiff") is a Texas limited liability company with its address at 6000 Shepherd Mountain Cove, Suite #1604, Austin, Texas 78730.

2. On information and belief, Defendant Airspan Networks Inc. ("Defendant" or "Airspan") is a corporation organized and existing under the laws of Delaware with a place of business at 777 Yamato Road, Suite 310, Boca Raton, FL 33431. Airspan has a registered agent, Patrica Durante, at 777 Yamato Road, Suite 310, Boca Raton, FL 33431.

II. JURISDICTION AND VENUE

3. This action arises under the patent laws of the United States, Title 35 of the United States Code. This Court has subject matter jurisdiction of such action under 28 U.S.C. §§ 1331 and 1338(a).

4. On information and belief, Defendant is subject to this Court's specific and general personal jurisdiction, pursuant to due process and the Florida Long-Arm Statute, due at least to its

business in this forum, including at least a portion of the infringements alleged herein at 777 Yamato Road, Suite 310, Boca Raton, FL 33431.

5. Without limitation, on information and belief, within this state, Defendant used the patented invention thereby committing acts of patent infringement alleged herein. In addition, on information and belief, Defendant derived revenues from its infringing acts that occurred within Florida. Further, on information and belief, Defendant is subject to the Court's general jurisdiction, including from regularly doing or soliciting business, engaging in other persistent courses of conduct, and deriving substantial revenue from goods and services provided to persons or entities in Florida. Further, on information and belief, Defendant is subject to the Court's personal jurisdiction at least due to its sale of products and/or services within Florida. Defendant committed such purposeful acts and/or transactions in Florida such that it reasonably should know and expect that it could be haled into this Court as a consequence of such activity.

6. Venue is proper in this district under 28 U.S.C. § 1400(b). On information and belief, Defendant is headquartered within this District at 777 Yamato Road, Suite 310, Boca Raton, FL 33431. On information and belief from and within this District, Defendant has committed at least a portion of the infringements at issue in this case.

7. For these reasons, personal jurisdiction exists and venue is proper in this Court under 28 U.S.C. § 1400(b).

III. COUNT I (PATENT INFRINGEMENT OF UNITED STATES PATENT NO. 6,813,742)

8. Plaintiff incorporates the above paragraphs herein by reference.

9. On November 2, 2004, the USPTO duly and legally issued U.S. Patent No. 6,813,742 ("the '742 Patent" or "Patent-in-Suit"), entitled "High Speed Turbo Codes Decoder for 3G Using Pipelined SISO Log-Map Decoders Architecture." The '742 patent was the subject of a

reexamination request filed on July 13, 2006. An *Ex Parte* Reexamination Certificate was issued for the '742 patent on February 10, 2009. A true and correct copy of the '742 Patent with its *Ex Parte* Reexamination Certificate is attached hereto as Exhibit 1.

10. TurboCode is the assignee of all right, title, and interest in the '742 patent, including all rights to enforce and prosecute actions for infringement and to collect damages for all relevant times against infringers of the '742 Patent. Accordingly, TurboCode possesses the exclusive right and standing to prosecute the present action for infringement of the '742 Patent by Defendant.

11. This case generally relates to decoder architectures and processes for receiving and decoding data in communications devices.

12. **Direct Infringement.** Upon information and belief, Defendant directly infringed claim 6 of the '742 Patent in Florida, and elsewhere in the United States, by performing actions comprising using or performing the claimed method of iteratively decoding a plurality of sequences of received baseband signals by using and/or testing products, devices, systems, and/or components of systems that comply with the 4G/LTE standards as disclosed in the 3rd Generation Partnership Project ("3GPP") Standard Specifications (releases 8-13 [while citations to release 8 are provided herein, the technical material is also found in releases 9-13]) governing cellular wireless communications (such standards also referred to as 4G/LTE) ("Accused Instrumentalities") and that were designed, developed, tested, used in the United States, or that have a nexus to the United States. The Accused Instrumentalities include at least the following Airspan products: Air Harmony 1000, Air Harmony 4000, Air Harmony 4200, Air Harmony 4400, Airspeed 1000, Airspeed 1030, Airspeed 1050, Airspeed 1250, Air Synergy, AiRU, AirSpot 1310, AirSpot 1412, AirSpot 5410, AirSpan GPS-ANT-3, Air4G, Airspot 430P, Airspan AirSpot ZT621, and Air Velocity 1500. The Accused Instrumentalities include the listed products (together with

support indicating that the identified product complies with relevant 4G/LTE standards and contains a baseband processor) and any products reasonably similar thereto (*e.g.*, products or model numbers marketed under a substantially similar name or that vary from a listed product by incorporating features that do not alter compliance with 4G/LTE standards).

13. Claim 6 of the '742 Patent *Ex Parte* Reexamination Certificate states:

> A method of iteratively decoding a plurality of sequences of received baseband signals, the method comprising:
>
> providing an input buffer comprising at least three shift registers, for receiving an input signal and generating first, second, and third shifted input signals;
>
> providing first and second soft decision decoders serially coupled in a circular circuit, wherein each decoder processes soft decision from the preceding decoder output data, and wherein the first decoder further receives the first and second shifted input signals from the input buffer and the second decoder further receives the third shifted input signal from the input buffer;
>
> providing at least one memory module coupled to an output of each of the first and second soft decision decoders, wherein the output of the memory module associated with the second soft decision decoder is fed back as an input of the first soft decision decoder;
>
> processing systematic information data and extrinsic information data using the maximum a posteriori (AP) probability algorithm, and/or logarithm approximation algorithm;
>
> generating soft decision based on the maximum a posteriori (MAP) probability algorithm, and/or logarithm approximation algorithm;
>
> weighing and storing soft decision information into the corresponding memory module;
>
> performing, for a predetermined number of times, iterative decoding from the first to the last of multiple decoders, wherein an output from the last soft decision decoder is fed back as an input to the first soft decision decoder, then from the first to the second decoders, and propagate to the last decoder in a circular circuit.

14. The Accused Instrumentalities performed (or were used by Defendant to perform) a method of iteratively decoding a plurality of sequences of received baseband signals, as shown

below by their compliance with the 4G/LTE standards (defined in the 3GPP Standard Specifications):

AirHarmony 1000 Outdoor 4G LTE eNodeB
Low Powered, With Wireline Backhaul Options

AirHarmony 1000 is a Compact and versatile 4G LTE Micro eNodeB that provides the outdoor Micro layer of a Heterogeneous LTE network deployment (HetNet). Supports 3GPP's latest LTE releases (software upgradeable). Support for SON and advanced interference mitigation techniques enabling N−1 frequency re-use with the Umbrella Macro cell. The cooperative QoS over the Backhaul interface ensures the QoE from the Micro eNodeB matches the experience from the Macro cell.

Plug and Play
Full plug-and-play functionality, out-of-the-box to fully operational, within 20 minutes.

The Power of HetNets
Ideal for networks, delivering high data rates and significant cell size where needed most.

Broadband Access
Supports the latest 3GPP LTE broadband access technologies.

Integrated Backhaul
Supports various backhaul options including multiple fiber / copper interfaces which allows for a variety of network topologies.

Latest Release LTE Feature Sets
Supports the latest 3GPP Release feature sets (software ugradeable). Also includes support for SON and eICIC which enables N−1 frequency re-use with the Umbrella Macro cell.

Reduced CAPEX/OPEX
Can be installed without conventional indoor infrastructure, associated power and air-conditioning.

Radio Planning with SON
Designed to integrate with a standardized LTE Access SON solution.

Need more information? Get in touch with the Airspan sales team by visiting airspan.com/contact.

(*E.g.*, https://airadio.com/download?file=mediaPool/u2G9oxJ.pdf).

AirHarmony 4000 Outdoor 4G LTE eNodeB
With Integrated Wireline Backhaul Options

AirHarmony 4000 is a Mini-Macro carrier-class LTE small cell eNodeB that supports 3GPP's latest LTE releases eNodeB specifications (software upgradeable). It provides high-speed data, mobility, Voice over LTE, and roadcast/ multicast services in order to meet the demands of fixed and mobile LTE carriers.

Plug and Play
Full plug-and-play functionality, out-of-the-box to fully operational, within 20 minutes.

The Power of HetNets
Ideal for networks, delivering high data rates and significant cell size where needed most.

Broadband Access
Supports the latest 3GPP LTE broadband access technologies.

Integrated Wireline Backhaul
Supports various backhaul options including multiple fiber / copper interfaces which allows for a variety of network topologies.

Latest Release LTE Feature Sets
Supports the latest 3GPP Release feature sets (software ugradeable). Also includes support for SON and eICIC which enables N=1 frequency re-use with the Umbrella Macro cell.

Reduced CAPEX/OPEX
Can be installed without conventional indoor infrastructure, associated power and air-conditioning.

Radio Planning with SON
Designed to integrate with a standardized LTE Access SON solution.

Need more information? Get in touch with the Airspan sales team by visiting airspan.com/contact.

(*E.g.*, https://airspan.com/wp-content/uploads/2024/01/AirHarmony-4000.pdf).

AirHarmony 4200 Outdoor 4G LTE eNodeB
With Integrated Wireline Backhaul Options

AirHarmony 4200 is a Mini-Macro carrier-class LTE small cell eNodeB that supports 3GPP's latest LTE releases eNodeB specifications (software upgradeable). It provides high-speed data, mobility, Voice over LTE, and roadcast/ multicast services in order to meet the demands of fixed and mobile LTE carriers.

Plug and Play
Full plug-and-play functionality, out-of-the-box to fully operational, within 20 minutes.

The Power of HetNets
Ideal for networks, delivering high data rates and significant cell size where needed most.

Broadband Access
Supports the latest 3GPP LTE broadband access technologies.

Integrated Wireline Backhaul
Supports various backhaul options including multiple fiber / copper interfaces which allows for a variety of network topologies.

Latest Release LTE Feature Sets
Supports the latest 3GPP Release feature sets (software ugradeable). Also includes support for SON and eICIC which enables N=1 frequency re-use with the Umbrella Macro cell.

Reduced CAPEX/OPEX
Can be installed without conventional indoor infrastructure, associated power and air-conditioning.

Radio Planning with SON
Designed to integrate with a standardized LTE Access SON solution.

Need more information? Get in touch with the Airspan sales team by visiting airspan.com/contact.

(*E.g.*, https://airadio.com/download?file=mediaPool/uwPQwpQ.pdf).

AirHarmony 4400 Outdoor 4G LTE eNodeB
With Integrated Wireline Backhaul Options

AirHarmony 4400 is a Mini-Macro carrier-class LTE small cell eNodeB that supports 3GPP's latest LTE releases eNodeB specifications (software upgradeable). It provides high-speed data, mobility, Voice over LTE, and broadcast multicast services in order to meet the demands of fixed and mobile LTE carriers.

Plug and Play
Full plug-and-play functionality, out-of-the-box to fully operational, within 20 minutes.

The Power of HetNets
Ideal for networks, delivering high data rates and significant cell size where needed most.

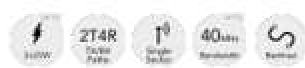
Broadband Access
Supports the latest 3GPP LTE broadband access technologies.

Integrated Wireline Backhaul
Supports various backhaul options including multiple fiber / copper interfaces which allows for a variety of network topologies.

Latest Release LTE Feature Sets
Supports the latest 3GPP Release feature sets (software ugradeable). Also includes support for SON and eICIC which enables N=1 frequency re-use with the Umbrella Macro cell.

Reduced CAPEX/OPEX
Can be installed without conventional indoor infrastructure, associated power and air-conditioning.

Radio Planning with SON
Designed to integrate with a standardized LTE Access SON solution.



Need more information? Get in touch with the Airspan sales team by visiting airspan.com/contact.

(*E.g.*, https://airadio.com/download?file=mediaPool/ulXNhSn.pdf).

AirHarmony 4400 is part of Airspan's carrier-class LTE Advanced small cell eNodeB family. AirHarmony 4400 is a Macro-class product that supports 3GPP's Long Term Evolution (LTE) eNodeB specifications, providing high-speed data, mobility, Voice over LTE, and broadcast/multicast services in order to meet the demands of the LTE Mobile Carriers.

AirHarmony 4400 is a compact, easy to install Macro-class eNodeB, allowing an operator to deploy LTE broadband services using existing infrastructure or Street Furniture. AirHarmony 4400 has two 20W (43dBm) transmit channels and four receive channels. AirHarmony 4400 supports single or dual carrier up to 2x 20MHz.

Release 10 LTE-Advanced

AirHarmony 4400 supports 3GPP LTE Broadband access technologies; Airspan's 3GPP LTE implementation is compliant with the 3GPP standards and has interoperable S1 and X2 interfaces and supports commercial GCF tested UE devices, including Smartphones, Dongles and Tablet computers.

(*E.g.*, https://teltech.com/wp-content/uploads/2023/07/Airspan-Spec-Sheets.pdf).

AirSpeed 1000 Outdoor Pico Small Cell

Dual Sector/Carrier Compact eNB

The AirSpeed 1000 is part of Airspan's carrier-class, LTE small cell, eNodeB family. It is a Pico class product that supports 3GPP's Long Term Evolution (LTE) eNodeB specifications, providing high-speed data, mobility, Voice over LTE, and broadcast/multicast services in order to meet the demands of the LTE fixed and Mobile Carriers.

Easy to Install
Single Mounting + Power only.

All Major LTE Bands Supported
Operates in LTE licensed and Lightly-licensed Bands.

Integrated Backhaul
Integrated wireline backhaul.

Various Deployment Scenarios
Compact form factor allows simple installation on rooftops, walls and poles.

High Coverage/Throughput
4T4R channels configured as dual sector with LiteCoMP, dual carrier*.

Enhanced AirSON
Fast commissioning and network configuration.

Latest Release LTE Feature Sets
Supports the latest 3GPP Release feature sets (software ugradeable). Also includes support for SON and eICIC which enables N=1 frequency re-use with the Umbrella Macro cell.

Need more information? Get in touch with the Airspan sales team by visiting airspan.com/contact.

(*E.g.*, https://airadio.com/download?file=mediaPool/ubrLbud.pdf).

AirSpeed 1030 Compact Outdoor Small Cell

With Dual Sector Smart Beam Antennas

The AirSpeed 1030 is part of Airspan's carrier-class, LTE small cell, eNodeB family. It is a high powered Pico class product with integrated dual sector front mount smart beam antennas that provides high-speed data, mobility, Voice over LTE, and broadcast/multicast services in order to meet the demands of the LTE fixed and Mobile Carriers.

Easy to Install
Single Mounting + Power only.

All Major LTE Bands Supported
Operates in LTE licensed and Lightly-licensed Bands.

Integrated Backhaul
Supports wireline backhaul options.

Various Deployment Scenarios
Compact form factor allows simple installation on rooftops, walls and poles.

High Coverage/Throughput
4T4R channels configured as dual sector with LiteCoMP, dual carrier*.

Enhanced AirSON
Fast commissioning and network configuration.

Latest Release LTE Feature Sets
Supports the latest 3GPP Release feature sets (software ugradeable). Also includes support for SON and eICIC which enables N−1 frequency re-use with the Umbrella Macro cell.

Need more information? Get in touch with the Airspan sales team by visiting airspan.com/contact.

(*E.g.*, https://airspan.com/products/4g/airspeed-1030/).

AirSpeed 1050 Compact Outdoor Small Cell

With Dual Sector Smart Beam Antennas

The AirSpeed 1050 is part of Airspan's carrier-class, LTE small cell, eNodeB family. It is a Pico class product that supports 3GPP's Long Term Evolution (LTE) eNodeB specifications, providing high-speed data, mobility, Voice over LTE, and broadcast/multicast services in order to meet the demands of the LTE fixed and Mobile Carriers.

Easy to Install
Single Mounting + Power only.

All Major LTE Bands Supported
Operates in LTE licensed and Lightly-licensed Bands.

Integrated Backhaul
Supports wireline backhaul options.

Various Deployment Scenarios
Compact form factor allows simple installation on rooftops, walls and poles.

High Coverage/Throughput
4T4R channels configured as dual sector with LiteCoMP, dual carrier*.

Enhanced AirSON
Fast commissioning and network configuration.

Latest Release LTE Feature Sets
Supports the latest 3GPP Release feature sets (software ugradeable). Also includes support for SON and eICIC which enables N=1 frequency re-use with the Umbrella Macro cell.

Need more information? Get in touch with the Airspan sales team by visiting airspan.com/contact.

(*E.g.*, https://airadio.com/download?file=mediaPool/ueLsr6w.pdf).

AirSpeed 1250 compact outdoor Pico-Cell

High Coverage with Integrated Relay Backhaul

EASY TO INSTALL
Single Mounting + Power only

ALL MAJOR LTE BANDS SUPPORTED
Operates in LTE licensed and Lightly-licensed Bands.

INTEGRATED BACKHAUL
Supports LTE Relay, DOCSIS, 60GHz and satellite or wireline backhaul options.

VARIOUS DEPLOYMENT SCENARIOS
Compact form factor allows simple installation on rooftops, walls and poles.

HIGH COVERAGE/ THROUGHPUT
4T4R channels configured as dual sector with LiteCoMP, dual carrier* or 4×4 MIMO*.

ENHANCED AIRSON
Fast commissioning and network configuration.

AirSpeed 1250

AirSpeed 1250 is an LTE-A (FDD or TDD) outdoor small cell with a wireless backhaul connection, and is used where wireline backhaul is not available or not feasible.
It can be mounted on walls and poles. AirSpeed is composed of an eNB for access, and a standard high-performance UE relay for wireless backhaul. Instead of connecting to the EPC via wireline backhaul, the eNB is connected directly to the UE relay, and the UE relay is connected via a standard LTE wireless connection to the Donor eNB.

(*E.g.*, https://www.scribd.com/document/426504553/Airspan-Pico-ENodeB).

2 Introduction

This section provides a descriptive overview of the Airspan's AirSynergy Pico eNodeB and its place in the product suite.

2.1 AirSynergy

AirSynergy is part of Airspan's carrier-class 4G Pico eNodeB family. AirSynergy supports 3GPP's Long Term Evolution (LTE) eNodeB, providing high-speed data and mobility, in order to meet the demands of the Broadband Wireless Access market.

AirSynergy is a compact, easy to install pico-cell, allowing an operator to deploy LTE broadband services using existing Street Furniture (e.g. street lamps, power poles, etc…)

(*E.g.*, https://manualzz.com/doc/38736475/airspan-airsynergy-2000-lte-base-station-installation-guide).

Air-Synergy

4G Pico Base Station with Integrated Wireless Backhaul

LTE SPECIFICATIONS

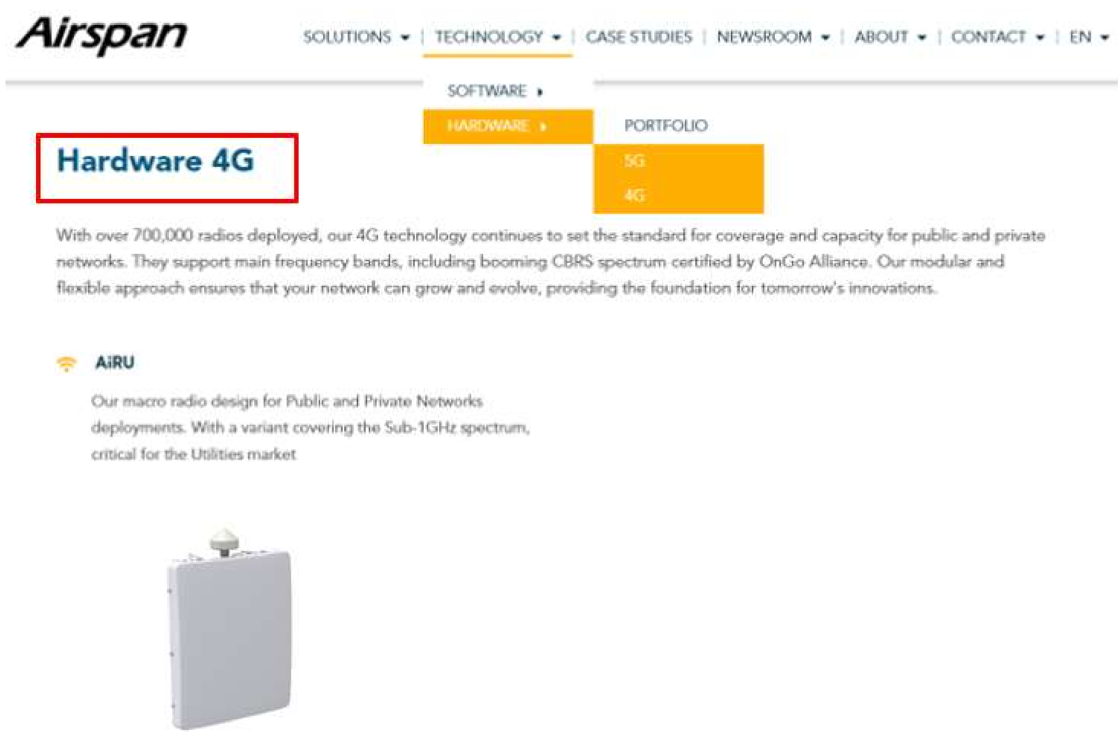
RADIO INTERFACE

Version:	Release 8/9 (10 in future)
Operational Frequency Bands:	2.3GHz 2.6GHz 3.5GHz 800MHz 700MHz
Duplex:	FDD & TDD
Max Channel BW:	10MHz (20MHz in future)
Max Transmit Power:	2 x +27dBm & 2x +30dBm options
MCS Support:	QPSK, 16QAM, 64QAM
Synchronisation:	GPS & IEEE1588

KEY FEATURES

Advanced Antenna Techniques	System Features
2x2 MIMO	Inter-RAT Mobility
SU-MIMO	RAN Sharing
MU-MIMO	Automatic Neighbour Relation (ANR)
	Inter-cell Interference Coordination

(*E.g.*, https://fcc.report/FCC-ID/O2J-365AS/1539957.pdf).



(*E.g.*, https://airspan.com/hardware/#4g).

Airspan

AirSpot 1310

DATASHEET

Add Coverage Outdoors

CAT6, LTE, Outdoor CPE

The AirSpot 1310 is an advanced, LTE, outdoor, CPE solution specifically designed to meet integrated data needs for residential, business, and enterprise users. It supports advanced Gigabit networking functionalities, and provides wide coverage, high-data throughput, and networking features to customers who need easy broadband access.

(*E.g.*, https://www.ispsupplies.com/core/media/media.nl?id=8102207&c=393682&h=chL0mn1SoLi5w6QRD9SKMDetw6c97pPoPh8sQKnH2v12px4Z).

Airspan

AirSpot 1412 is a highly advanced LTE outdoor multi-service product solution specifically designed to meet integrated data needs for residential, business and enterprise users. The product supports advanced Gigabit networking functionalities. It enables wide service coverage and provides high data throughput and networking features to customers who need easy broadband access.

(*E.g.*, https://manualzz.com/download/64053756).

Airspan

Airspan AirSpot 5410 LTE ODU,B42H,43L,48,C12,PoE,US plug, For CBRS only

(*E.g.*, https://www.ispsupplies.com/Airspan-My-Pro-FC-B42H-43L-48-C12-CB).

Airspan

CPE-CBSD
AirSpot 5410
DATASHEET

Easy and Reliable Wireless Broadband Access
CPE-CBSD, Rugged, CAT12, 18 dBi Outdoor CPE

Part of Airspan's end-to-end CBRS solution, the AirSpot 5410 is an advanced, LTE, CAT12, outdoor, multi-service product specifically designed to meet data needs for residential, business and enterprise users. Supporting Gigabit networking functionality and multiple TDD band operations, it enables wide-coverage and high-data throughput. Multiple operator network support can allow deployment across the country with different operators. The AirSpot 5410 provides a Gigabit PoE connection to connect user terminal devices, such as a router or WiFi AP products. It is CAT-B CBSD FCC and SAS compliant.

Rugged and Reliable
Built for the outdoors, with an IP67 rating, it can safely operate in temperatures ranging from -40° to 65° C.

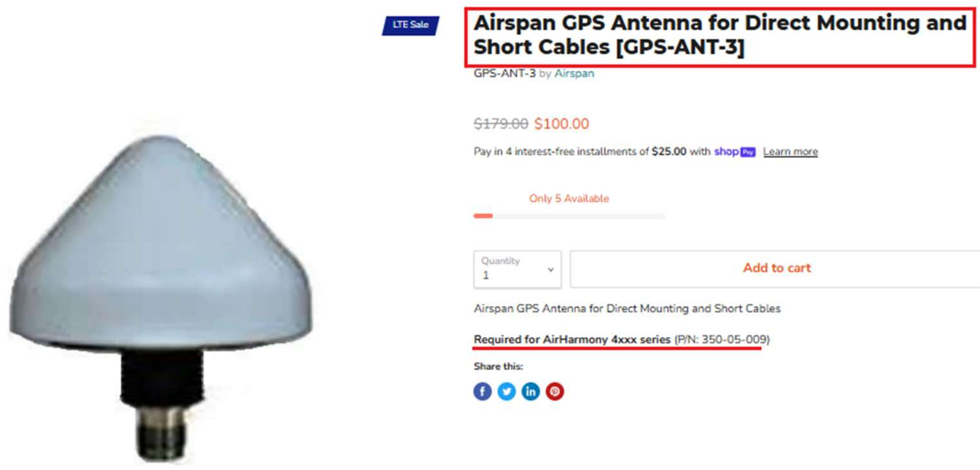
High Performance
Depending on the configuration and traffic split, the unit can provide up to 600 Mbps download speeds and increased cell edge with its internal, high-gain, 18 dBi antennas.

Easy to Use
Once connected to a CBSD, simply connect it to a computer, switch or router, and it's ready to go. Eight LED's easily communicate the status, and IP addresses are dynamically obtained via its internal DHCP.

Easy to Manage
Supports local management access, Telnet, HTTP, HTTPS and standard TR069 remote OTA management, including device configuration, monitoring, and upgrades management. Firmware upgrades can be done from a pre-configured URL using HTTP/FTP.

Advanced Technology
Based on 3GPP standard implementation of LTE CAT12 specifications, it can easily meet requirements of large service providers. Supports up to 4CA DL and 2CA UL, MIMO capabilities, 64QAM modulation (uplink), and 256QAM modulation (downlink).

(*E.g.*, https://www.ispsupplies.com/core/media/media.nl?id=9384275&c=393682&h=AIe8glh7n62sf5xzk7vL7kzZ70fwijj3zfcvXQ6l921WPP2s).



(*E.g.*, https://www.balticnetworks.com/products/airspan-gps-antenna-for-direct-mounting-and-short-cables-p-n-350-05-009-33-3012-01-01?_pos=2&_sid=584f2e66a&_ss=r&_fid=df29d1224).

Air 4G is interoperable with end devices of all form factors, based on all leading chips. It is also interoperable with various core network solutions.

LTE SPECIFICATIONS

RADIO INTERFACE

3GPP Version:	Release 8/9 (10 in future)
Operational Frequency Bands:	700 MHz 2.3 – 2.4 GHz 2.496 – 2.7 GHz 3.3 – 3.8 GHz *Including E-UTRA operating bands #7, 17, 38, 40 and 41*
Duplex:	FDD & TDD
Channel BW:	1.4 MHz, 3 MHz, 5 MHz, 10 MHz, 15 MHz, 20 MHz
Max Transmit Power:	2 x +40 dBm, 4 x 37 dBm
MCS Support:	QPSK, 16-QAM, 64-QAM
Synchronization:	GPS & IEEE1588

KEY FEATURES

Advanced Antenna Techniques

- 2 x 2 MIMO
- SU-MIMO
- MU-MIMO

System Features

- Inter-RAT Mobility
- RAN Sharing
- Automatic Neighbor Relation (ANR)
- Inter-cell Interference Coordination

(*E.g.*, https://www.4gon.co.uk/documents/airspan_air4g_brochure.pdf).

Airspot 430P LTE Outdoor CPE

About this item

Seller assumes all responsibility for this listing.

Last updated on Oct 01, 2024 12:08:38 PDT View all revisions

Item specifics

Condition	New: A brand-new, unused, unopened, undamaged item in its original packaging (where packaging is ... Read more	Brand	AirSpan
Type	CPE	Model	430P
MPN	999-03-649	Product Line	LTE
UPC	Does not apply		

(*E.g.*, https://www.amazon.com/-/es/Airspot-430P-LTE-Outdoor-CPE/dp/B091B93DYR).

Airspan AirSpot ZT621 - 2.5 GHz / Band 38 41 Category 12 LTE UE CPE

About this item

Item specifics

Condition	New: A brand-new, unused, unopened, undamaged item in its original packaging (where packaging is ... Read more	Maximum LAN Data Rate	1000 Mbps
Network Connectivity	Wired-Ethernet (RJ-45)	Custom Bundle	No
Color	White	Ports	Ethernet (RJ-45)
MPN	999-03-723-US, My-Pro-ZM-838-841-C02	Modified Item	No
Brand	Airspan	Type	LTE UE
Cellular Network Technology	LTE	Manufacturer Warranty	None
Model	AirSpot ZT621	Connectivity	Wired-Ethernet (RJ-45), 4G
Features	Unlocked	Carrier	Band 38/41 - 2.5GHz
Country/Region of Manufacture	China	Number of LAN Ports	1
Wireless Standard	4G LTE	UPC	Does not apply

(*E.g.*, https://www.ebay.com/itm/133991337400).

AirVelocity 1500

High Speed Indoor LTE Small Cell

Ideal for public venues and offices

AirVelocity is a revolutionary indoor, high performance, LTE-Advanced small cell, designed to bring Public Access LTE networks to indoor spaces. AirVelocity reduces the indoor mobile hot spots and creates much greater indoor coverage for end users. AirVelocity is one of the key solutions for CBRS deployments, with FCC certification

AirVelocity 1500 Product Specification

Revision: 1.6

(*E.g.*, https://www.scribd.com/document/771949089/AirVelocity-1500-Product-Specification-Rev1-6).

8. LTE Radio Performance

8.1. Frequency Stability

The AirVelocity 1500 reference frequency accuracy is better than ±0.05ppm.

8.2. Modulation & FEC

AirVelocity 1500 supports QPSK, 16QAM and 64QAM modulations on both Downlink and Uplink with all Modulation and Coding Schemes defined in 3GPP TS 36.211.

8.3. Frame Durations & Cyclic Prefixes

8.3.1. Frame Duration

AirVelocity 1500 supports 10ms frames, as well as 1ms subframes, as defined by 3GPP.

8.3.2. Cyclic Prefix

The following Cyclic Prefixes (CP) are used:

TABLE 6: AIRVELOCITY 1500 CYCLIC PREFIXES FOR LTE

Subcarrier Spacing (KHz)	Normal CP (us)	Extended CP (us)
15	~5.2 for first DFT block ~4.7 for remaining DFT blocks	16.7

(*E.g.*, https://www.scribd.com/document/771949089/AirVelocity-1500-Product-Specification-Rev1-6).

AirVelocity 1500

High Speed Indoor LTE Small Cell

Ideal for public venues and offices

AirVelocity is a revolutionary indoor, high performance, LTE-Advanced small cell, designed to bring Public Access LTE networks to indoor spaces. AirVelocity reduces the indoor mobile hot spots and creates much greater indoor coverage for end users. AirVelocity is one of the key solutions for CBRS deployments, with FCC certification

(*E.g.*, https://airspan.com/products/4g/airvelocity-1500/).

15. The Accused Instrumentalities performed (or were used to perform) a method of iteratively decoding a plurality of sequences of received baseband signals in accordance with the 4G/LTE standards disclosed in the applicable 3GPP Standard Specifications.

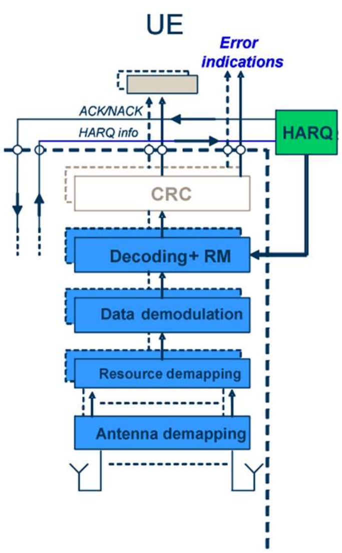


Figure 6.2.1-1: Physical-layer model for DL-SCH transmission

(*See* 3GPP TS 36.302 at 12 (v. 8))

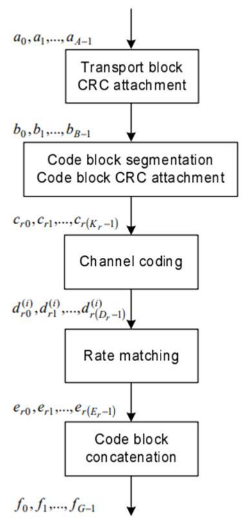


Figure 5.3.2-1: Transport channel processing for DL-SCH, PCH and MCH

(*See* 3GPP TS 36.212 at 37 (v. 8))

5 Channel coding, multiplexing and interleaving

Data and control streams from/to MAC layer are encoded /decoded to offer transport and control services over the radio transmission link. Channel coding scheme is a combination of error detection, error correcting, rate matching, interleaving and transport channel or control information mapping onto/splitting from physical channels.

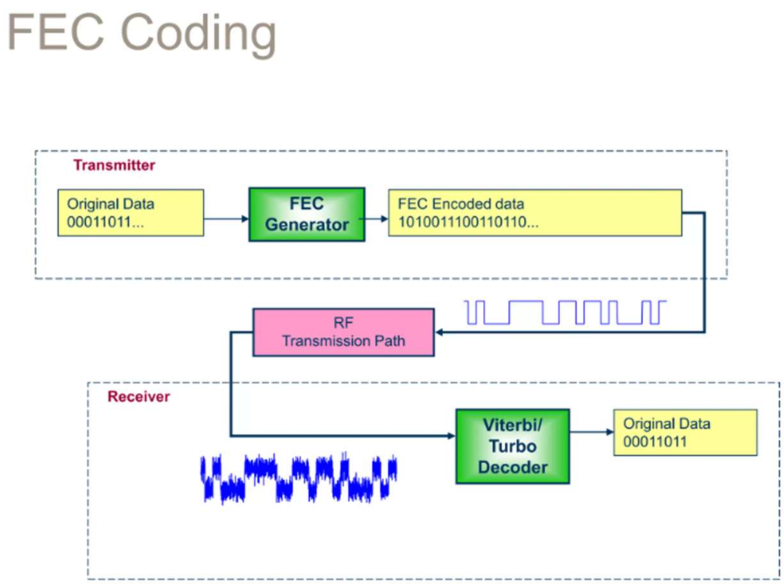
The following channel coding schemes can be applied to TrCHs:

- tail biting convolutional coding;
- turbo coding.

Table 5.1.3-1: Usage of channel coding scheme and coding rate for TrCHs

TrCH	Coding scheme	Coding rate
UL-SCH	Turbo coding	1/3
DL-SCH		
PCH		
MCH		

(*See* 3GPP TS 36.212 at 37 (v. 8)).



(*See* https://www.slideshare.net/slideshow/lte-air-interface-71056106/71056106).

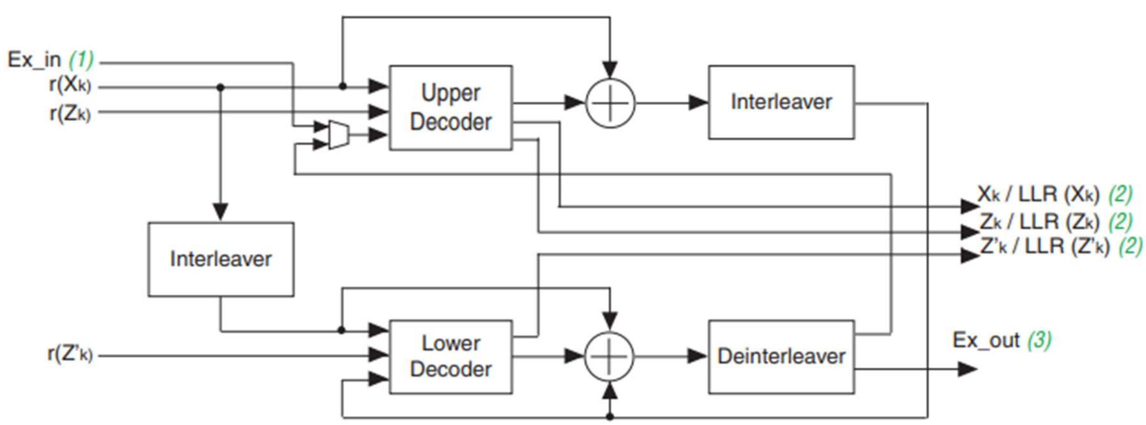
Description

The LTE Turbo Decoder block implements the turbo decoder required by LTE standard TS 36.212 [1] and provides an interface and architecture optimized for HDL code generation and hardware deployment. The block iterates over two MAX decoders. You can specify the number of iterations. The coding rate is 1/3. The block accepts encoded bits as a 3-by-1 vector of soft-coded values, `[S P1 P2]`. In this vector, `S` is the systematic bit, and `P1` and `P2` are the parity bits from the two encoders.

(*See* https://www.mathworks.com/help/wireless-hdl/ref/lteturbodecoder.html).

Turbo Decoder

Figure 3. Turbo Decoder Architecture



16. The Accused Instrumentalities provided (or were used to provide) (*e.g.*, via an input buffer) input to the constituent decoders of the turbo decoder. The input buffer comprises at least three shift registers. The input buffer receives an input signal, and first, second, and third shifted

input signals are generated for input to a turbo decoder. The generated first, second, and third shifted input signals, shown as "x_k output at encoder," "z_k output at encoder" and "z'_k *and* x'_k output at encoder" are input into the upper decoder and 2nd constituent decoder as shown below:

> "5.1.3.2.1 Turbo encoder
>
> The scheme of turbo encoder is a Parallel Concatenated Convolutional Code (PCCC) with two 8-state constituent encoders and one turbo code internal interleaver. The coding rate of turbo encoder is 1/3. The structure of turbo encoder is illustrated in figure 5.1.3-2.
>
> The initial value of the shift registers of the 8-state constituent encoders shall be all zeros when starting to encode the input bits."
>
> …
>
> The bits input to the turbo encoder are denoted by $c_0, c_1, c_2, c_3, ..., c_{K-1}$, and the bits output from the first and second 8-state constituent encoders are denoted by $z_0, z_1, z_2, z_3, ..., z_{K-1}$ and $z'_0, z'_1, z'_2, z'_3, ..., z'_{K-1}$, respectively. The bits output from the turbo code internal interleaver are denoted by $c'_0, c'_1, ..., c'_{K-1}$, and these bits are to be the input to the second 8-state constituent encoder."

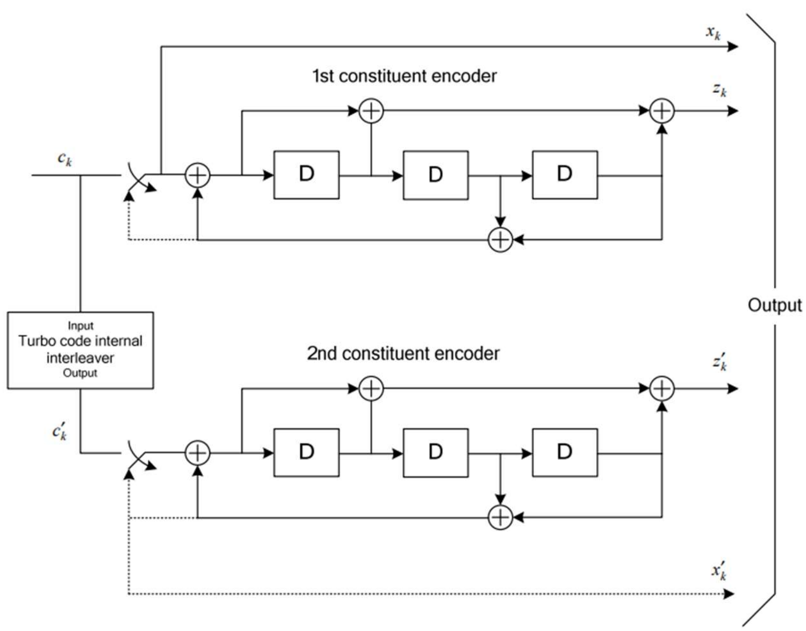
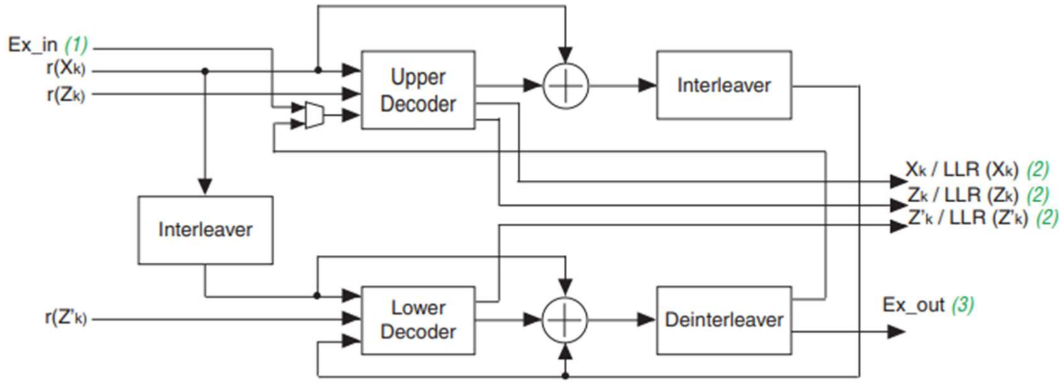


Figure 5.1.3-2: Structure of rate 1/3 turbo encoder (dotted lines apply for trellis termination only)

(*See* 3GPP TS 36.212 at 13, 14 (v. 8)).

Figure 3. Turbo Decoder Architecture



> "Double-buffering supports reduced latency real-time applications by allowing the decoder to receive data while processing the previous data block."

(*See* Altera Corporation, "3GPP LTE Turbo Reference Design" (Jan. 2020), *available at* https://www.intel.com/content/dam/www/programmable/us/en/pdfs/literature/an/an505.pdf Page 7, 8 ("A Turbo decoder consists of two single soft-in soft-out (SISO) decoders, which work iteratively.")).

17. Each such buffer provides three sections based on operations of a turbo encoder. For example, an input buffer is denoted as Figure 5.1.4-1, labeled as a "Rate matching for turbo coded transport channels":

> 5.1.4 Rate matching
>
> 5.1.4.1 Rate matching for DL-SCH and UL-SCH
>
> The rate matching for DL-SCH and UL-SCH is defined per coded block and consists of interleaving the three information bit streams, $d_k^{(0)}$, $d_k^{(1)}$ and $d_k^{(2)}$, followed by the collection of bits and the generation of a circular buffer as depicted in Figure 5.1.4-1. The output bits for each code block are transmitted as described in subclause 5.1.4.1.2.

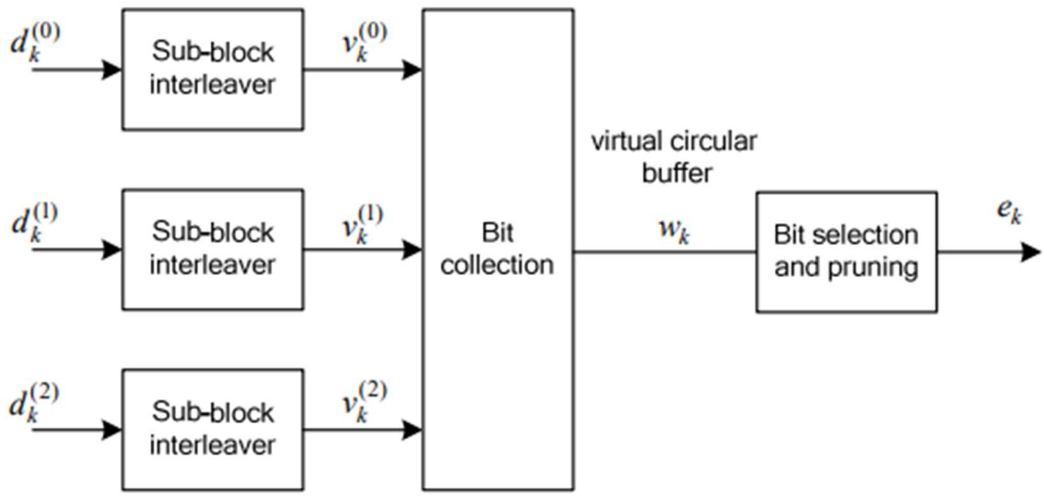


Figure 5.1.4-1. Rate matching for turbo coded transport channels

(*See* 3GPP TS 36.212, at 16, 18 (v. 8)).

> 5.1.3.2.2 Trellis termination for turbo encoder
>
> Trellis termination is performed by taking the tail bits from the shift register feedback after all information bits are encoded. Tail bits are padded after the encoding of information bits.

(*See* 3GPP TS 36.212, at 16 (v. 8)). Such a channel coded bit buffer can then be decoded using shifting to generate the first, second, and third shifted input signals, which are stored in registers for input into the turbo decoder. *See also Cheng et. al.* "A 0.077 to 0.168 nj/bit/iteration Scalable 3GPP LTE Turbo Decoder with an Adaptive Sub-Block Parallel Scheme and an Embedded DVFS Engine," 2010 IEEE Custom Integrated Circuits Conference (CICC) (19-22 Sept. 2010), at Fig. 3, *available at* https://dspace.mit.edu/bitstream/handle/1721.1/72198/Chandrakasan-a%200.077%20to%200.168.pdf?sequence=1&isAllowed=y

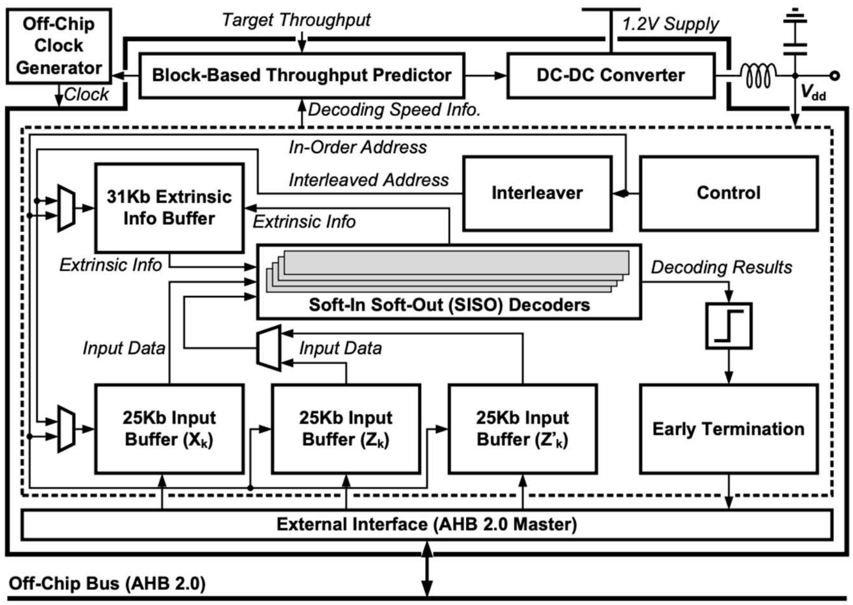
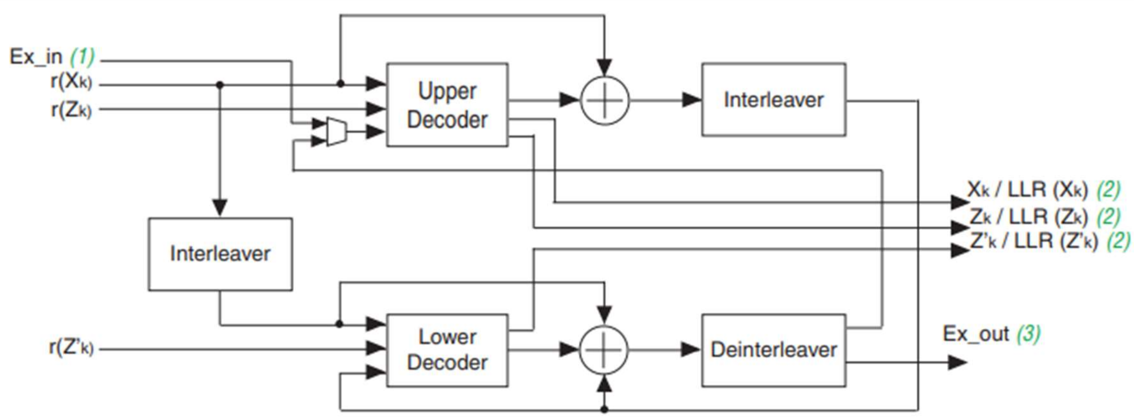


Fig. 3. The system architecture.

18. Additionally, each of the Accused Instrumentalities processed (or were used to process) received baseband digital signals in an iterative manner through its implementation of turbo decoding. The turbo decoder implementation receiving and operating on an incoming input signal includes an input buffer structure and three component shift registers to provide time-aligned values (i.e., first, second, and third shifted input signals) needed for each SISO computation. To the extent that any of the Accused Instrumentalities does not implement shift register functions in hardware, it is a well-established convention to implement shift register functions via software. (*See, e.g.,* Wikipedia, "Shift register," *available at* https://en.wikipedia.org/wiki/Shift_register ("Many computer languages include instructions to 'shift right' and 'shift left' the data in a register, effectively dividing by two or multiplying by two for each place shifted."); GeeksforGeeks, "Left Shift and Right Shift Operators in C/C++," *available at* https://www.geeksforgeeks.org/left-shift-right-shift-operators-c-cpp/; mbedded.ninja, "Shift Registers," §5 (Apr. 8, 2020), *available at* https://blog.mbedded.ninja/electronics/components/shift-registers/).

19. The Accused Instrumentalities provided (or were used to provide) first and second soft decision decoders serially coupled in a circular circuit, wherein each decoder processes soft decision from the preceding decoder output data, and wherein the first decoder further receives the first and second shifted input signals from the input buffer and the second decoder further receives the third shifted input signal from the input buffer. *See, e.g.,* Altera Corporation, "3GPP LTE Turbo Reference Design" (Jan. 2020), *available at* https://www.intel.com/content/dam/www/programmable/us/en/pdfs/literature/an/an505.pdf Page 7, 8 ("A Turbo decoder consists of two single soft-in soft-out (SISO) decoders, which work iteratively.").

Figure 3. Turbo Decoder Architecture



In the example, the first upper decoder outputs a soft decision that goes through an "interleaver" to become upper decoder output. This "upper decoder output" is fed as input into the lower decoder, for the second decision decoder to process. The second lower decoder also receives the " z'_k " input signal. The lower decoder outputs soft decision that becomes "lower decoder output" after exiting "deinterleaver." This "lower decoder output" is fed as input into the upper decoder

for the upper decoder to process. The upper decoder, "1st constituent decoder," also receives the "x_k" and "z_k" input signals.

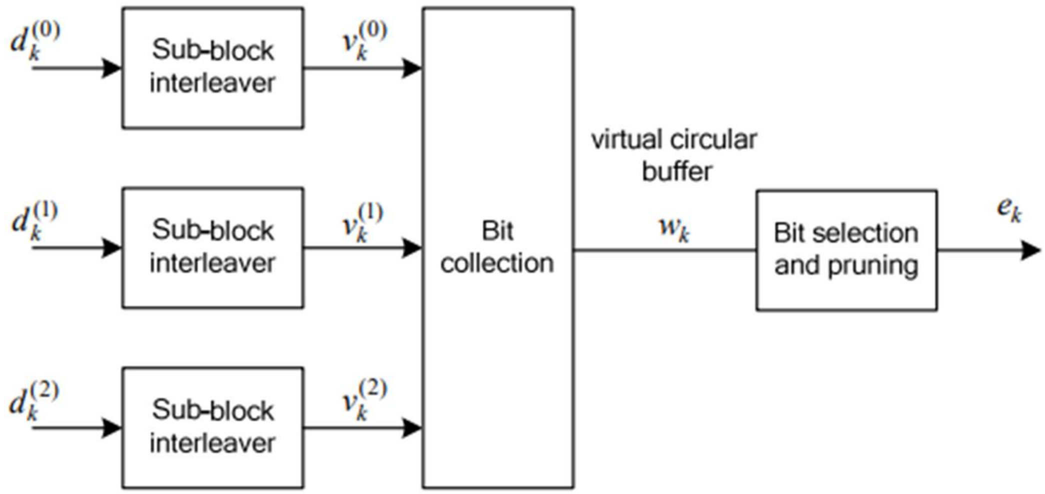


Figure 5.1.4-1. Rate matching for turbo coded transport channels

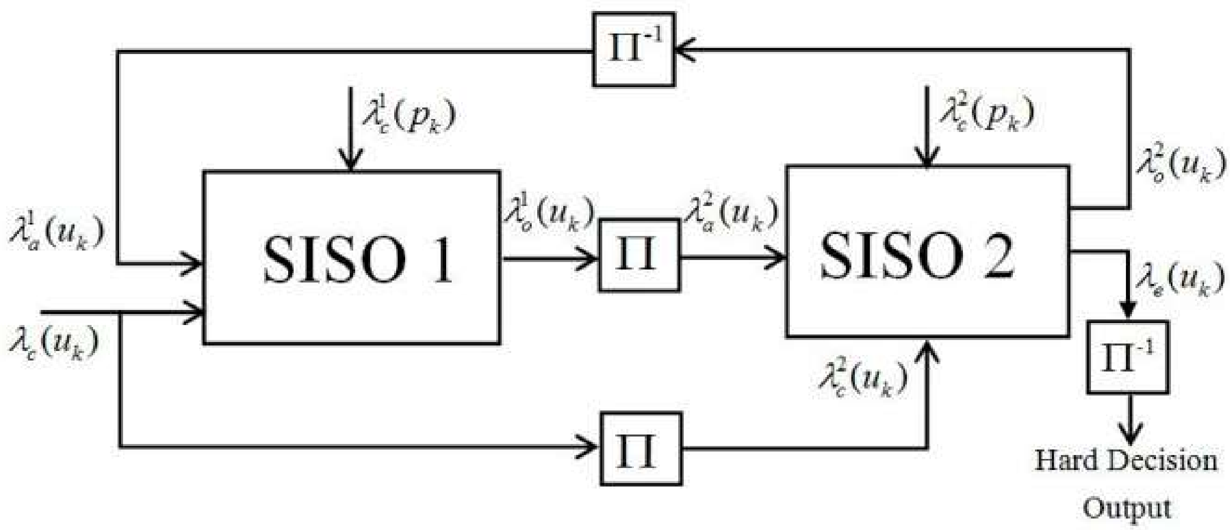
(*See* 3GPP TS 36.212, at 16, 18 (v. 8)).

> 5.1.3.2.2 Trellis termination for turbo encoder
>
> Trellis termination is performed by taking the tail bits from the shift register feedback after all information bits are encoded. Tail bits are padded after the encoding of information bits.

(*Id.*). *See also Cheng et. al.* "A 0.077 to 0.168 nj/bit/iteration Scalable 3GPP LTE Turbo Decoder with an Adaptive Sub-Block Parallel Scheme and an Embedded DVFS Engine," 2010 IEEE Custom Integrated Circuits Conference (CICC) (19-22 Sept. 2010), at 3, *available at* https://dspace.mit.edu/bitstream/handle/1721.1/72198/Chandrakasan-a%200.077%20to%200.168.pdf?sequence=1&isAllowed=y:

> "Figure 3 shows the system architecture. The blocks in the dashed box handle the turbo decoding operations, and those outside the dashed box belong to the DVFS scheme. Turbo decoding is an iterative process with several turbo iterations. Each turbo iteration comprises two soft-in, soft-out (SISO) decoding processes using BCJR algorithm [8] with the first one performed on the input code block in the original order and the second one in an order generated by the interleaver block."

20. Additionally, as explained above, all known commercial implementations of 4G LTE turbo decoders are iterative and functionally equivalent to the figure below. The figure below illustrates soft decision from the preceding decoder output (a posteriori information) being fed as an input (a priori information) in an iterative mode. The top of the figure below illustrates the feedback loop that forces 4G LTE turbo decoders to be iterative. The iterative loop traverses elements SISO 1, Π, SISO 2, Π^{-1}, and closes with the signal path return to the input of SISO 1 to form a circular circuit.

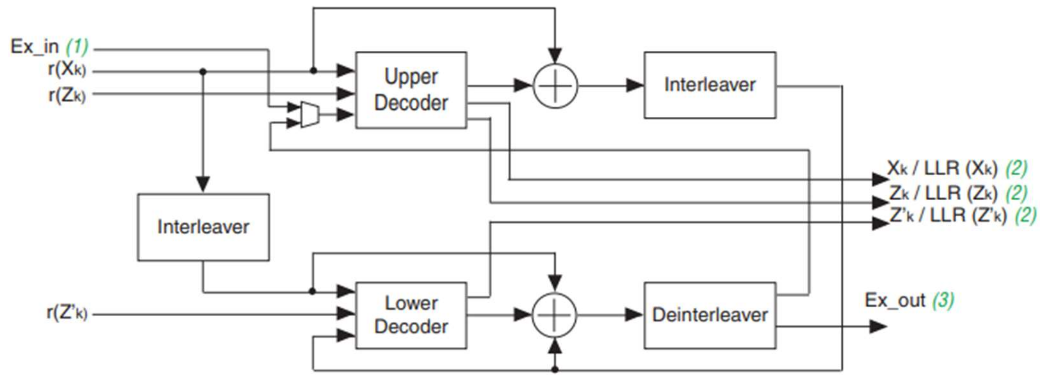


(*See* Jun Li et al., "Turbo Decoder Design based on an LUT-Normalized Log-MAP Algorithm," Entropy (Basel) (Aug. 20, 2019), *available at* https://www.ncbi.nlm.nih.gov/pmc/articles/PMC7515343/ ("The SISO decoder consists of three input ports, which are system information $\lambda_c(u_k)$, parity information $\lambda_c(p_k)$, and a priori information $\lambda_a(u_k)$ which is computed by another SISO decoder. Two output ports of the SISO decoder generate external information $\lambda_e(u_k)$ and posteriori information $\lambda_o(u_k)$. The different superscripts represent information corresponding to different SISO decoders, and subscript *k* denotes *k*-th bit information of the current variable.")).

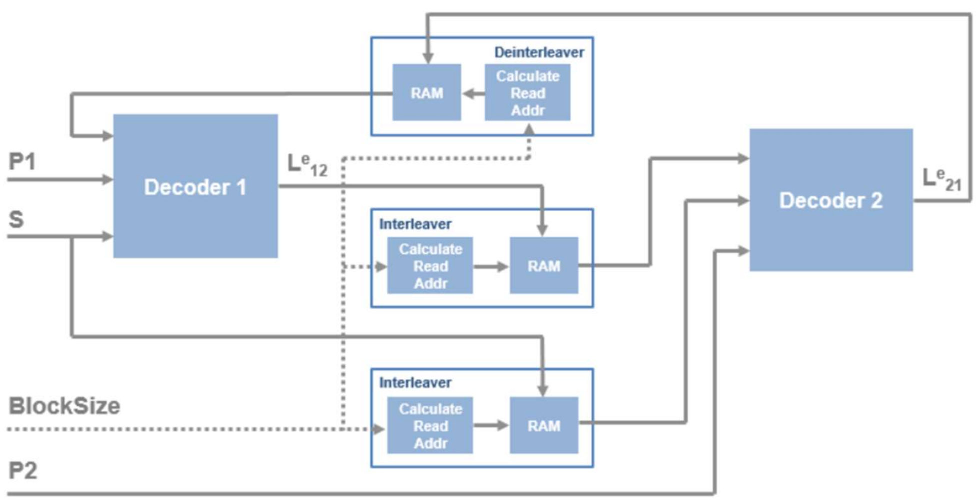
21. As explained above, each of the Accused Instrumentalities processed (or were used to process) received baseband digital signals in an iterative manner through its implementation of turbo decoding. The turbo decoder implementation receiving and operating on an incoming input signal includes an input buffer structure and three component shift registers to provide time-aligned values (*i.e.*, first, second, and third shifted input signals) needed for each SISO computation. To the extent that any of the Accused Instrumentalities does not implement shift register functions in hardware, it is a well-established convention to implement shift register functions via software. *See, e.g.,* Wikipedia, "Shift register," *available at* https://en.wikipedia.org/wiki/Shift_register ("Many computer languages include instructions to 'shift right' and 'shift left' the data in a register, effectively dividing by two or multiplying by two for each place shifted."); GeeksforGeeks, "Left Shift and Right Shift Operators in C/C++," *available at* https://www.geeksforgeeks.org/left-shift-right-shift-operators-c-cpp/; mbedded.ninja, "Shift Registers," §5 (Apr. 8, 2020), *available at* https://blog.mbedded.ninja/electronics/components/shift-registers/.

22. The Accused Instrumentalities included at least one memory module (*e.g.*, "interleaver" to the right of the "upper decoder" and "deinterleaver" in the figure below), that is electrically coupled to an output of a corresponding soft decision decoder (*e.g.*, "upper decoder" and "lower decoder")), wherein the output of the memory module associated with the second soft decision decoder ("deinterleaver") is fed back as an input of the first soft decision decoder, as shown below:

Figure 3. Turbo Decoder Architecture



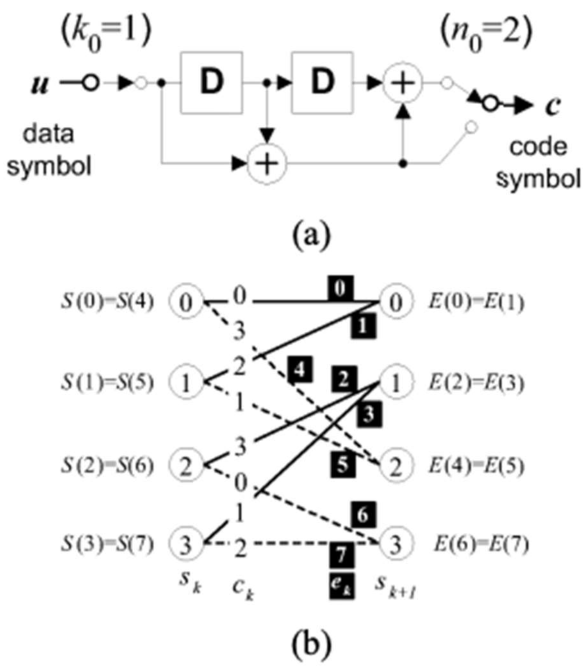
(*See,* Altera Corporation, "3GPP LTE Turbo Reference Design" (Jan. 2020), *available at* https://www.intel.com/content/dam/www/programmable/us/en/pdfs/literature/an/an505.pdf Page 7, 8 ("A Turbo decoder consists of two single soft-in soft-out (SISO) decoders, which work iteratively.")). In the example, the "deinterleaver" memory module is associated with the second soft decision decoder, "lower decoder." The output of the deinterleaver, "deinterleaver output," is fed back as an input of the first soft decision decoder, "upper decoder." These "interleaver" and "deinterleaver" comprise memory modules. (*See* "LTE Turbo Decoder", *available at* (https://ww2.mathworks.cn/help/wireless-hdl/ref/lteturbodecoder.html)).



See also Mansour et al., "VLSI Architectures for SISO-APP Decoders," IEEE Transactions On Very Large Scale Integration ("VLSI") Systems, Vol. 11, No. 4 (Aug. 2003):

> "Fig. 1. A (2, 1, 3) convolutional code. (a) An encoder with 2 memory delay elements (D) and modulo 2 adders, data symbol alphabet {0, 1}, code symbol alphabet {0, 1, 2, 3}, memory states {0, 1, 2, 3}, and code rate R = (1=2). (b) A trellis section where solid edges correspond to u = 0, and dashed edges correspond to u = 1. The output code symbols c are shown on the edges. The edges are numbered with black squares, and the edge starting and ending states are shown on the left and right, respectively."

See also id. at FIG. 1:



(*See also Cheng et. al.* "A 0.077 to 0.168 nj/bit/iteration Scalable 3GPP LTE Turbo Decoder with an Adaptive Sub-Block Parallel Scheme and an Embedded DVFS Engine," 2010 IEEE Custom Integrated Circuits Conference (CICC) (19-22 Sept. 2010), at Fig. 3, *available at* https://dspace.mit.edu/bitstream/handle/1721.1/72198/Chandrakasan-a%200.077%20to%200.168.pdf?sequence=1&isAllowed=y).

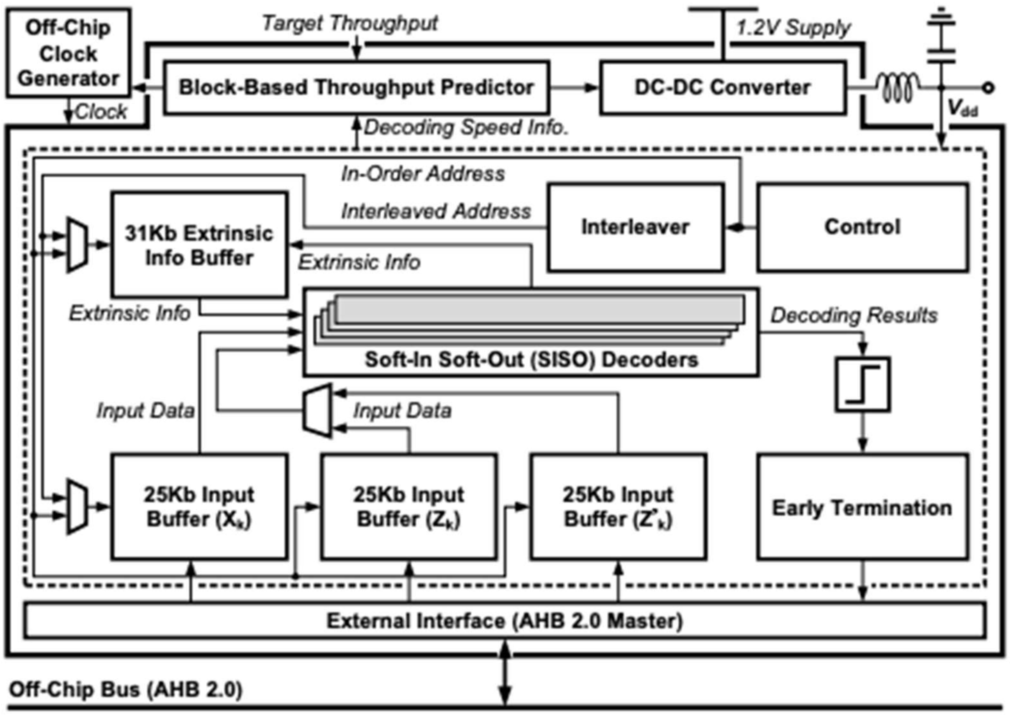
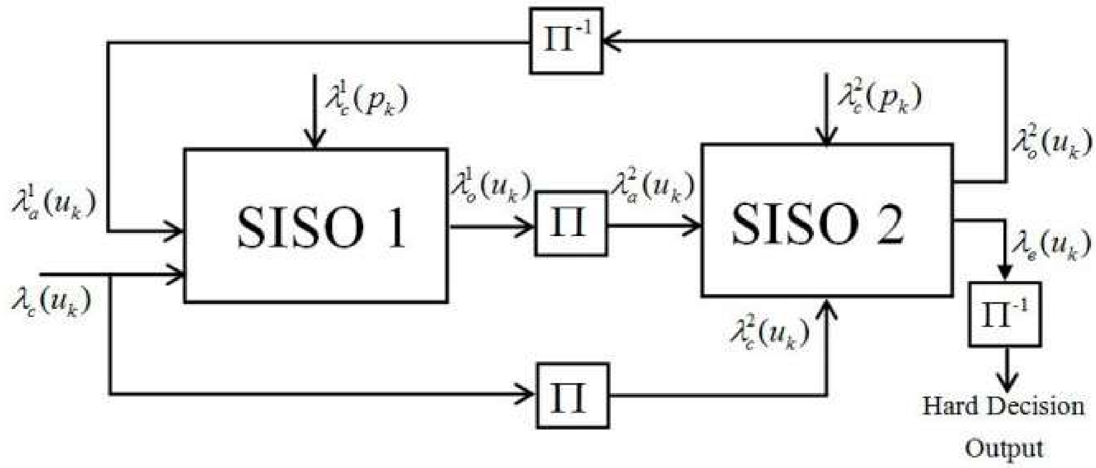


Fig. 3. The system architecture.

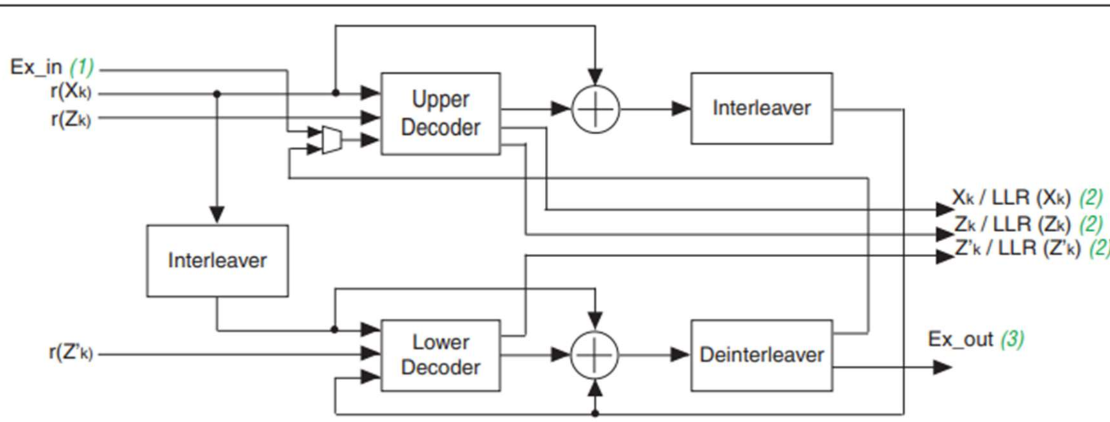
Additionally, as explained above, all known commercial implementations of 4G LTE turbo decoders are iterative and functionally equivalent to the figure below. The figure below illustrates output of the memory module associated with a last soft decision decoder fed back as an input to the first soft decision decoder via interleaving and/or de-interleaving (*e.g.*, the a posteriori output of SISO 2 is de-interleaved with the associated memory module and fed back as a priori input of SISO 1).



See Jun Li et al., "Turbo Decoder Design based on an LUT-Normalized Log-MAP Algorithm," Entropy (Basel) (Aug. 20, 2019), *available at* https://www.ncbi.nlm.nih.gov/pmc/articles/PMC7515343/ ("Π and Π−1 denote interleaving and de-interleaving, respectively.").

23. The Accused Instrumentalities processed (or were used to process) systematic information data and extrinsic information data using the maximum a posteriori (MAP) probability algorithm, and/or logarithm approximation algorithm. For example, the LTE Turbo Reference design decoder generally supports two variants of the Maximum A Posteriori (MAP) decoding algorithm:

Figure 3. Turbo Decoder Architecture



> "Decoding Algorithms The following two variants of the Maximum A Posteriori (MAP) decoding algorithm are supported:
>
> ■ LogMAP—Works on the logarithm domain of MAP and gives good bit error rate (BER) but consumes more logic resources. This option is currently not fully supported. Contact Altera for more information.
>
> ■ MaxLogMAP—A simplified version of LogMAP that uses less logic resource at a cost of slightly reduced BER performance relative to the LogMAP variant. The MaxLogMAP algorithm implemented in this reference design is a version of MaxLogMAP corrected with a scaling factor."

(*See,* Altera Corporation, "3GPP LTE Turbo Reference Design" (Jan. 2020), *available at* https://www.intel.com/content/dam/www/programmable/us/en/pdfs/literature/an/an505.pdf Page 7, 8 ("A Turbo decoder consists of two single soft-in soft-out (SISO) decoders, which work iteratively.")).

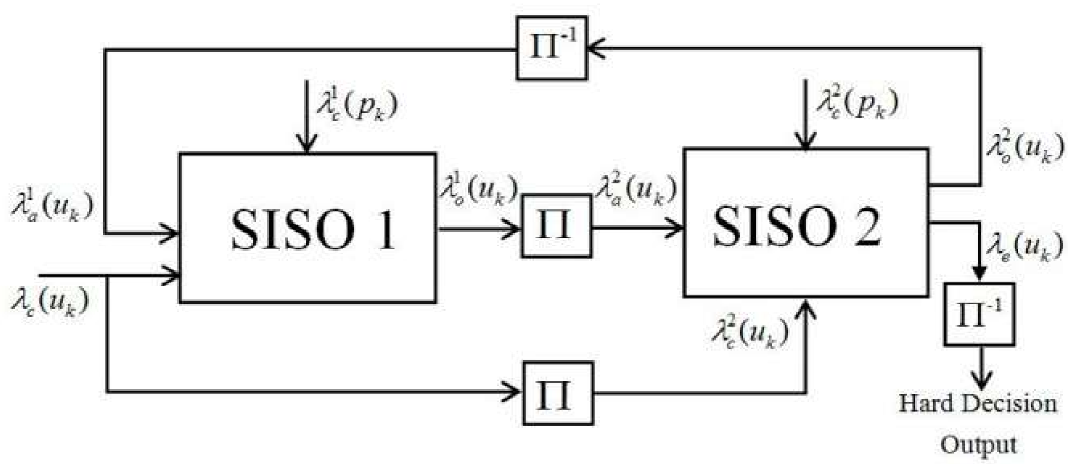
24. In another example, BCJR algorithm is a variant of MAP probability algorithm that processes systematic information data and extrinsic information data:

> "Turbo codes are composed of an interconnection of component codes through interleavers, typically convolutional codes, and their decoders consist of an equal number of component decoders each of which operates on its corresponding codeword and shares information with other component decoders iteratively according to the topology of the encoder. The decoding algorithm in the component decoders is the maximum a-posteriori probability (MAP) algorithm typically implemented in the form known as the Bahl–Cocke–Jelinek–Raviv (BCJR) algorithm [6]. The main advantage of a MAP decoding algorithm over a maximum likelihood decoding algorithm such as the Viterbi algorithm [7] is that it produces optimum soft information which is crucial to the operation of these decoders. The BCJR algorithm was generalized in [8] into a soft-input soft-output a posteriori probability (SISO-APP) algorithm to be used as a building block for iterative decoding in code networks with generic topologies. The advantages of the SISO-APP algorithm over other forms of the MAP algorithm is that it is independent of the code type (systematic/nonsystematic, recursive/nonrecursive, trellis with multiple edges), and it generates reliability information for code symbols as well as message symbols which makes it applicable irrespective of the concatenation scheme (parallel/serial/hybrid), and hence will be considered in this paper."

(*See* Mansour et al., "VLSI Architectures for SISO-APP Decoders," IEEE Transactions On Very Large Scale Integration ("VLSI") Systems, Vol. 11, No. 4 (Aug. 2003), at 627, *available at*

http://shanbhag.ece.illinois.edu/publications/mansr-tvlsi-2003-2.pdf; *See also id.* at 629 ("The decoding problem can now be defined as follows: given a noisy version of $\underline{c}$ denoted by $\underline{y}=\Delta(y_1,\cdots,y_k,\cdots,y_L)$, find the data sequence $\underline{u}$. There are two probabilistic solutions to this decoding problem. Maximum likelihood (ML) decoding determines the most likely connected path $\underline{s}$ through the trellis that maximizes the probability $P(\underline{y}|\underline{s})$. From $\underline{s}$, the most likely data sequence $\underline{u}$ is easily determined using (1). On the other hand, MAP decoding, which we consider here, determines $\underline{u}$ by estimating each of the symbols u_k independently using the observations $\underline{y}$. The kth estimated symbol u_k is the one that maximizes the posterior probability $P(u_k|\underline{y})$, and hence the name symbol-by-symbol MAP. The SISO-APP algorithm, a generalized version of the BCJR-APP algorithm [6], is a probabilistic algorithm that solves the MAP decoding problem.")).

25. Additionally, as explained above, all known commercial implementations of 4G/LTE turbo decoders are iterative and functionally equivalent to the figure below. The figure below illustrates that each decoder processes systemic information data and extrinsic information data—system information $\lambda_c(u_k)$, parity information $\lambda_c(p_k)$, a priori information $\lambda_a(u_k)$ and external information $\lambda_e(u_k)$.

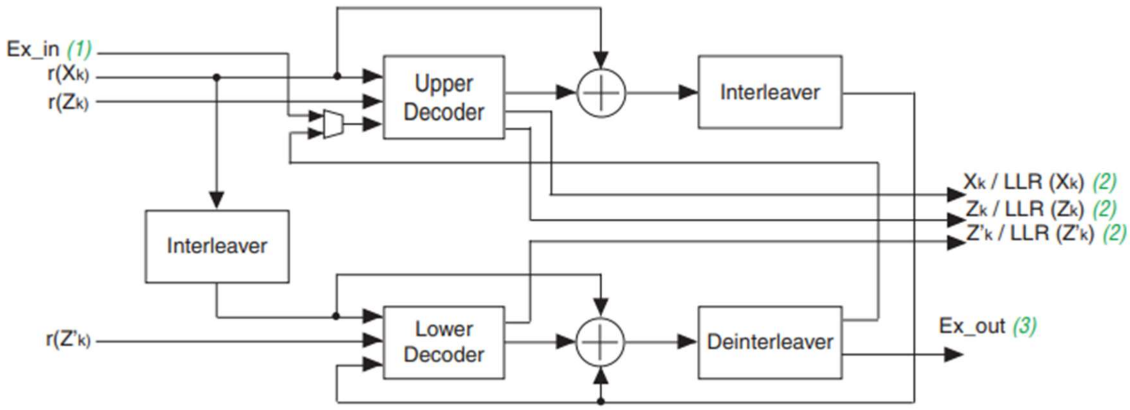


(*See* Jun Li et al., "Turbo Decoder Design based on an LUT-Normalized Log-MAP Algorithm," Entropy (Basel) (Aug. 20, 2019), *available at*

https://www.ncbi.nlm.nih.gov/pmc/articles/PMC7515343/. *See also, e.g.*, Guohui Wang *et al.*, "High-throughput Contention-Free Concurrent Interleaver Architecture for Multi-standard Turbo Decoder," ASAP 2011—22nd IEEE International Conference on Application-specific Systems, Architectures and Processors 113 (Sept. 2011); Cristian Anghel et al., "CTC Turbo Decoding Architecture for LTE Systems Implemented on FPGA," ICN 2012: The Eleventh International Conference on Networks 199, 199-200 (2012)). Each soft decision decoder on all known commercial implementations of any turbo decoder processed systematic information data and extrinsic information data using a maximum a posteriori (MAP) probability algorithm and/or a logarithm approximation algorithm to yield posteriori information $\lambda_o(u_k)$. (*See* Jun Li et al., "Turbo Decoder Design based on an LUT-Normalized Log-MAP Algorithm," Entropy (Basel) (Aug. 20, 2019), *available at* https://www.ncbi.nlm.nih.gov/pmc/articles/PMC7515343/ (discussing use of a log maximum a posteriori decoding algorithm); *see also, e.g.*, Guohui Wang *et al.*, "High-throughput Contention-Free Concurrent Interleaver Architecture for Multi-standard Turbo Decoder," ASAP 2011—22nd IEEE International Conference on Application-specific Systems, Architectures and Processors 113 (Sept. 2011) (noting that MAP decoders are used as the component SISO decoders); Cristian Anghel *et al.*, "CTC Turbo Decoding Architecture for LTE Systems Implemented on FPGA," ICN 2012: The Eleventh International Conference on Networks 199, 200 (2012) (describing ideal use of classic MAP algorithm and practical implementation of log-MAP algorithms)).

26. The Accused Instrumentalities generated (or were used to generate) soft decision based on the maximum a posteriori (MAP) probability algorithm and/or logarithm approximation algorithm. For example, the Accused Instrumentalities used at least the MAP algorithm for decoding in accordance with the figure below:

Figure 3. Turbo Decoder Architecture



> "Decoding Algorithms The following two variants of the Maximum A Posteriori (MAP) decoding algorithm are supported:
>
> ■ LogMAP—Works on the logarithm domain of MAP and gives good bit error rate (BER) but consumes more logic resources. This option is currently not fully supported. Contact Altera for more information.
>
> ■ MaxLogMAP—A simplified version of LogMAP that uses less logic resource at a cost of slightly reduced BER performance relative to the LogMAP variant. The MaxLogMAP algorithm implemented in this reference design is a version of MaxLogMAP corrected with a scaling factor."

(*See,* Altera Corporation, "3GPP LTE Turbo Reference Design" (Jan. 2020), *available at* https://www.intel.com/content/dam/www/programmable/us/en/pdfs/literature/an/an505.pdf Page 7, 8 ("A Turbo decoder consists of two single soft-in soft-out (SISO) decoders, which work iteratively.")). The relevant standards bodies, such as ETSI, provide technical articles that specify virtually all aspects of turbo encoders (i.e., turbo-code transmitters), turbo decoders (i.e., turbo-code receivers). The generic structure of a Soft Input Soft Output (SISO) Turbo decoder interconnected through an interleaver and a deinterleaver uses BCJR algorithm. The LTE Turbo decoder block uses the BCJR algorithm to find the likelihood ratio of a particular bit.

> "Annex E: Detailed Review of State-of-the-Art Error Correcting Codes E.1 Turbo Codes Turbo Codes (TC), were introduced in [i.123], where a systematic encoder consisting of two parallel concatenated recursive convolutional encoders separated by a bit interleaver, was proposed. Optimal decoding of this code is practically impossible, as the number of states in the trellis grow exponentially not only with

the convolutional encoder's memory, but also with the interleaver's length. However, the big innovation in the TC proposal was the possibility of suboptimal decoding with tractable complexity. The parallel concatenation of two BCJR algorithms [i.124] based on Soft Input Soft Output (SISO) decoders interconnected through an interleaver and a deinterleaver allowed performance as close as 0,7 dB (at BER =10-5) to the Shannon performance bound, after a small number of iterations. The very high coding gains offered by the turbo encoder can be credited to the combination of its various features. Indeed, although in conventional convolutional coding recursive encoders offer no benefits compared to non-recursive schemes, in TC recursive encoders have a great influence on the error probability as they introduce an interleaver gain [i.125]. The serial concatenation (separated by interleaving) of recursive convolutional encoders was proposed in [i.126] and has been established as the serial counterpart of the original parallel turbo encoder. Once again, crucial for the performance of the code is the recursive nature of the constituent encoders.

…

The generic structure of the Turbo decoder is illustrated in figure E-2. In the initial iteration Soft-Input-Soft-Output (SISO) decoder 1 accepts the channel observations of the code bit sequences that correspond to the systematic and first code branches.

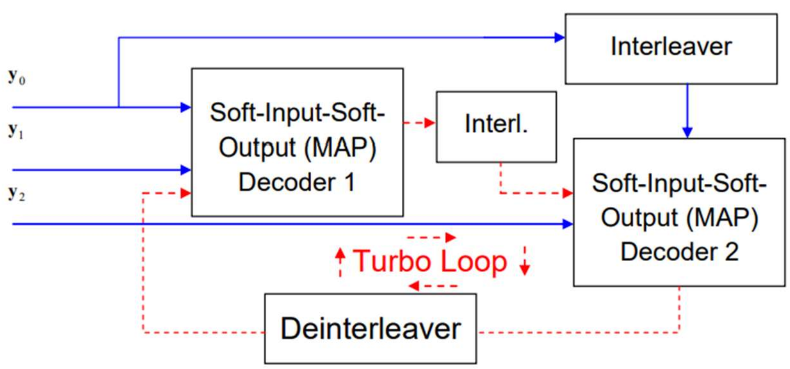


Figure E.2: Turbo Decoder

(*See* ETSI Technical Report on "Advanced satellite based scenarios and architectures for beyond 3G systems" (available at https://www.etsi.org/deliver/etsi_tr/102600_102699/102662/01.01.01_60/tr_102662v010101p.pdf Page 108, 109).

LTE Turbo Decoder

Description

The LTE Turbo Decoder block implements the turbo decoder required by LTE

> standard TS 36.212 [1] and provides an interface and architecture optimized for HDL code generation and hardware deployment. The block iterates over two MAX decoders. You can specify the number of iterations. The coding rate is 1/3. The block accepts encoded bits as a 3-by-1 vector of soft-coded values, [S P1 P2]. In this vector, S is the systematic bit, and P1 and P2 are the parity bits from the two encoders.
>
> …
>
> Algorithms
>
> The LTE Turbo Decoder block implements the turbo decoder required by LTE standard TS 36.212 [1] and provides an interface and architecture optimized for HDL code generation and hardware deployment. The block iterates over two MAX decoders. You can specify the number of iterations. The coding rate is 1/3. The block accepts encoded bits as a 3-by-1 vector of soft-coded values, [S P1 P2]. In this vector, S is the systematic bit, and P1 and P2 are the parity bits from the two encoders.
>
> …
>
> The decoder block uses the BCJR algorithm to find the likelihood ratio of a particular bit [2]."

(*See*, https://ww2.mathworks.cn/help/wireless-hdl/ref/lteturbodecoder.html).

27. In another example, BCJR algorithm is a variant of MAP probability algorithm that processes systematic information data and extrinsic information data to generate soft decision:

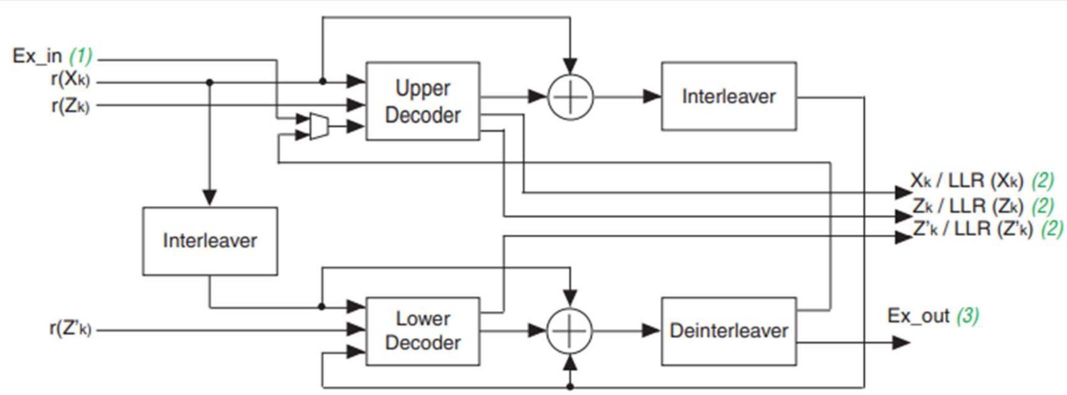
> "Turbo codes are composed of an interconnection of component codes through interleavers, typically convolutional codes, and their decoders consist of an equal number of component decoders each of which operates on its corresponding codeword and shares information with other component decoders iteratively according to the topology of the encoder. The decoding algorithm in the component decoders is the maximum a-posteriori probability (MAP) algorithm typically implemented in the form known as the Bahl–Cocke–Jelinek–Raviv (BCJR) algorithm [6]. The main advantage of a MAP decoding algorithm over a maximum likelihood decoding algorithm such as the Viterbi algorithm [7] is that it produces optimum soft information which is crucial to the operation of these decoders. The BCJR algorithm was generalized in [8] into a soft-input soft-output a posteriori probability (SISO-APP) algorithm to be used as a building block for iterative decoding in code networks with generic topologies. The advantages of the SISO-APP algorithm over other forms of the MAP algorithm is that it is independent of the code type (systematic/nonsystematic, recursive/nonrecursive, trellis with multiple edges), and it generates reliability information for code symbols as well as message symbols which makes it applicable irrespective of the concatenation

scheme (parallel/serial/hybrid), and hence will be considered in this paper."

(*See* Mansour et al., "VLSI Architectures for SISO-APP Decoders," IEEE Transactions On Very Large Scale Integration ("VLSI") Systems, Vol. 11, No. 4 (Aug. 2003), at 627, *available at* http://shanbhag.ece.illinois.edu/publications/mansr-tvlsi-2003-2.pdf; *see also id.* at 629 ("The decoding problem can now be defined as follows: given a noisy version of $\underline{c}$ denoted by $\underline{y}=\Delta(y_1,\cdots,y_k,\cdots,y_L)$, find the data sequence $\underline{u}$. There are two probabilistic solutions to this decoding problem. Maximum likelihood (ML) decoding determines the most likely connected path $\underline{s}$ through the trellis that maximizes the probability $P(\underline{y}|\underline{s})$. From $\underline{s}$, the most likely data sequence $\underline{u}$ is easily determined using (1) On the other hand, MAP decoding, which we consider here, determines $\underline{u}$ by estimating each of the symbols u_k independently using the observations $\underline{y}$. The kth estimated symbol u_k is the one that maximizes the posterior probability $P(u_k|\underline{y})$, and hence the name symbol-by-symbol MAP. The SISO-APP algorithm, a generalized version of the BCJR-APP algorithm [6], is a probabilistic algorithm that solves the MAP decoding problem.")).

28. The Accused Instrumentalities weighed and stored (or were used to weigh and store) soft decision information into the corresponding memory module (*e.g.*, "interleaver" or "deinterleaver") as shown in the figure below:

Figure 3. Turbo Decoder Architecture



(*See,* Altera Corporation, "3GPP LTE Turbo Reference Design" (Jan. 2020), *available at* https://www.intel.com/content/dam/www/programmable/us/en/pdfs/literature/an/an505.pdf Page 7 ("A Turbo decoder consists of two single soft-in soft-out (SISO) decoders, which work iteratively.")). The relevant standards bodies, such as ETSI, provide technical articles that specify virtually all aspects of turbo encoders (i.e., turbo-code transmitters), turbo decoders (i.e., turbo-code receivers). The generic structure of a Soft Input Soft Output (SISO) Turbo decoder interconnected through an interleaver and a deinterleaver uses BCJR algorithm. The LTE Turbo decoder block uses the BCJR algorithm to find the likelihood ratio of a particular bit.

> "Annex E: Detailed Review of State-of-the-Art Error Correcting Codes E.1 Turbo Codes Turbo Codes (TC), were introduced in [i.123], where a systematic encoder consisting of two parallel concatenated recursive convolutional encoders separated by a bit interleaver, was proposed. Optimal decoding of this code is practically impossible, as the number of states in the trellis grow exponentially not only with the convolutional encoder's memory, but also with the interleaver's length. However, the big innovation in the TC proposal was the possibility of suboptimal decoding with tractable complexity. The parallel concatenation of two BCJR algorithms [i.124] based on Soft Input Soft Output (SISO) decoders interconnected through an interleaver and a deinterleaver allowed performance as close as 0,7 dB (at BER =10-5) to the Shannon performance bound, after a small number of iterations. The very high coding gains offered by the turbo encoder can be credited to the combination of its various features. Indeed, although in conventional convolutional coding recursive encoders offer no benefits compared to non-recursive schemes, in TC recursive encoders have a great influence on the error probability as they introduce an interleaver gain [i.125]. The serial concatenation (separated by interleaving) of recursive convolutional encoders was proposed in [i.126] and has been established as the serial counterpart of the original parallel turbo encoder. Once again, crucial for the performance of the code is the recursive nature of the constituent encoders.
>
> …
>
> The generic structure of the Turbo decoder is illustrated in figure E-2. In the initial iteration Soft-Input-Soft-Output (SISO) decoder 1 accepts the channel observations of the code bit sequences that correspond to the systematic and first code branches."

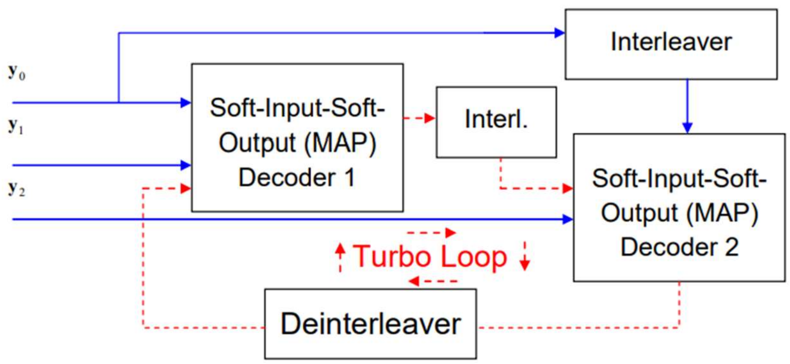


Figure E.2: Turbo Decoder

See ETSI Technical Report on *"*Advanced satellite based scenarios and architectures for beyond 3G systems"(available at https://www.etsi.org/deliver/etsi_tr/102600_102699/102662/01.01.01_60/tr_102662v010101p.pdf Page 108, 109.

> "LTE Turbo Decoder
>
> Description
>
> The LTE Turbo Decoder block implements the turbo decoder required by LTE standard TS 36.212 [1] and provides an interface and architecture optimized for HDL code generation and hardware deployment. The block iterates over two MAX decoders. You can specify the number of iterations. The coding rate is 1/3. The block accepts encoded bits as a 3-by-1 vector of soft-coded values, [S P1 P2]. In this vector, S is the systematic bit, and P1 and P2 are the parity bits from the two encoders.
>
> …
>
> Algorithms
>
> The LTE Turbo Decoder block implements the turbo decoder required by LTE standard TS 36.212 [1] and provides an interface and architecture optimized for HDL code generation and hardware deployment. The block iterates over two MAX decoders. You can specify the number of iterations. The coding rate is 1/3. The block accepts encoded bits as a 3-by-1 vector of soft-coded values, [S P1 P2]. In this vector, S is the systematic bit, and P1 and P2 are the parity bits from the two encoders.
>
> …
>
> The decoder block uses the BCJR algorithm to find the likelihood ratio of a

> particular bit [2]."

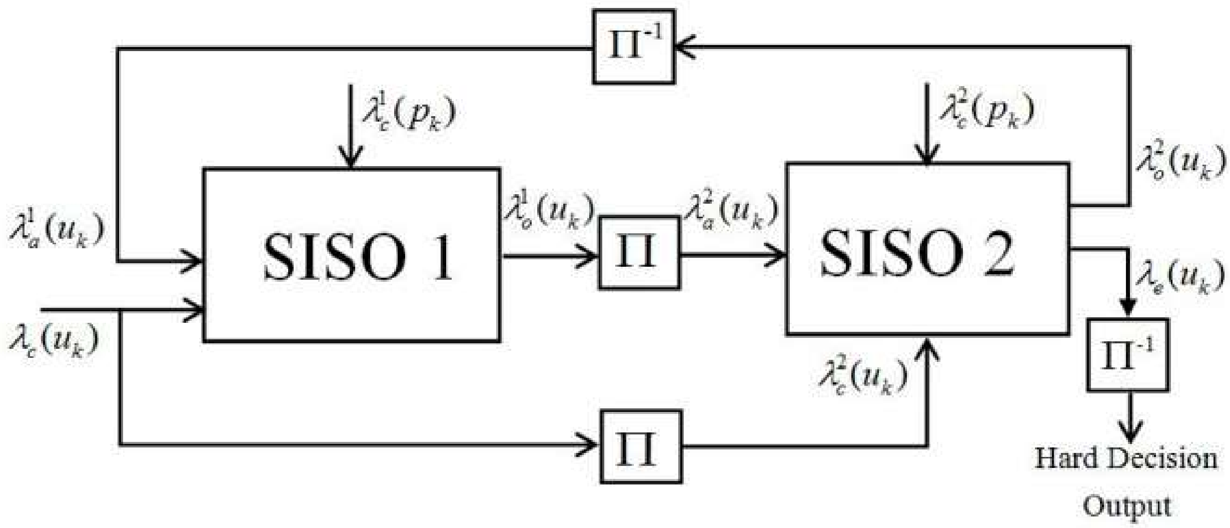
(*See*, https://ww2.mathworks.cn/help/wireless-hdl/ref/lteturbodecoder.html).

29. In another example, BCJR algorithm is a variant of MAP probability algorithm that processes systematic information data and extrinsic information data to generate soft decision:

> "Turbo codes are composed of an interconnection of component codes through interleavers, typically convolutional codes, and their decoders consist of an equal number of component decoders each of which operates on its corresponding codeword and shares information with other component decoders iteratively according to the topology of the encoder. The decoding algorithm in the component decoders is the maximum a-posteriori probability (MAP) algorithm typically implemented in the form known as the Bahl–Cocke–Jelinek–Raviv (BCJR) algorithm [6]. The main advantage of a MAP decoding algorithm over a maximum likelihood decoding algorithm such as the Viterbi algorithm [7] is that it produces optimum soft information which is crucial to the operation of these decoders. The BCJR algorithm was generalized in [8] into a soft-input soft-output a posteriori probability (SISO-APP) algorithm to be used as a building block for iterative decoding in code networks with generic topologies. The advantages of the SISO-APP algorithm over other forms of the MAP algorithm is that it is independent of the code type (systematic/nonsystematic, recursive/nonrecursive, trellis with multiple edges), and it generates reliability information for code symbols as well as message symbols which makes it applicable irrespective of the concatenation scheme (parallel/serial/hybrid), and hence will be considered in this paper."

(*See* Mansour et al., "VLSI Architectures for SISO-APP Decoders," IEEE Transactions On Very Large Scale Integration ("VLSI") Systems, Vol. 11, No. 4 (Aug. 2003), at 627, *available at* http://shanbhag.ece.illinois.edu/publications/mansr-tvlsi-2003-2.pdf).

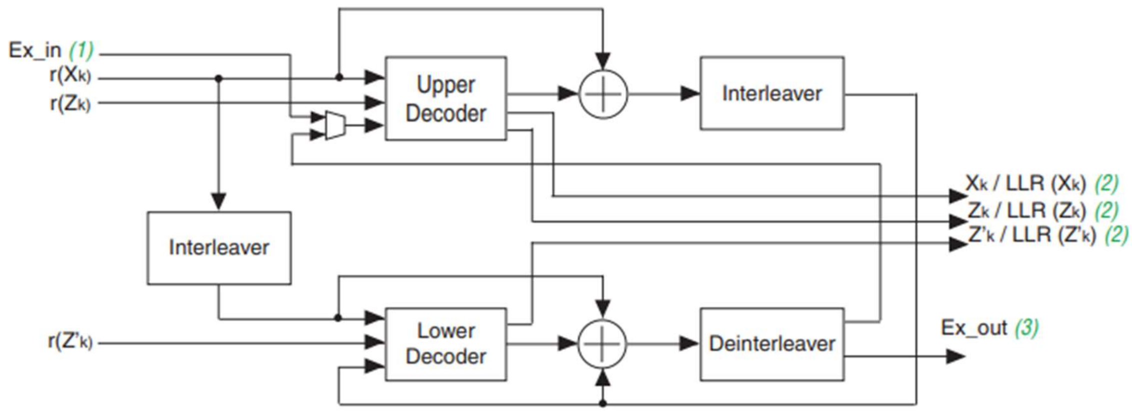
30. Additionally, as explained above, all known commercial implementations of 4G LTE turbo decoders are iterative and functionally equivalent to the figure below. The figure below illustrates that soft decision information is stored in the corresponding memory module (*e.g.*, the a posteriori output of SISO 1 is stored in the associated interleaver memory module Π, while the a posteriori output of SISO 2 is stored in the associated de-interleaver memory module Π^{-1}).



(*See* Jun Li et al., "Turbo Decoder Design based on an LUT-Normalized Log-MAP Algorithm," Entropy (Basel) (Aug. 20, 2019), *available at* https://www.ncbi.nlm.nih.gov/pmc/articles/PMC7515343/). On information and belief, use of any viable maximum a posteriori (MAP) probability algorithm and/or logarithm approximation algorithm necessarily requires weighing (or "normalization"); *see* Jun Li et al., "Turbo Decoder Design based on an LUT-Normalized Log-MAP Algorithm," Entropy (Basel) (Aug. 20, 2019), *available at* https://www.ncbi.nlm.nih.gov/pmc/articles/PMC7515343/ (discussing use of a log maximum a posteriori decoding algorithm); *see also, e.g.*, Guohui Wang *et al.*, "High-throughput Contention-Free Concurrent Interleaver Architecture for Multi-standard Turbo Decoder," ASAP 2011—22nd IEEE International Conference on Application-specific Systems, Architectures and Processors 113 (Sept. 2011) (noting that MAP decoders are used as the component SISO decoders); Cristian Anghel et al., "CTC Turbo Decoding Architecture for LTE Systems Implemented on FPGA," ICN 2012: The Eleventh International Conference on Networks 199, 200 (2012) (describing ideal use of classic MAP algorithm and practical implementation of log-MAP algorithms)).

31. The Accused Instrumentalities performed (or were used to perform) for a predetermined number of times, iterative decoding from the first to the last of multiple decoders, wherein an output from the last soft decision decoder is fed back as an input to the first soft decision decoder, then from the first to the second decoders, and propagate to the last decoder in a circular circuit, as shown in the figure below:

Figure 3. Turbo Decoder Architecture



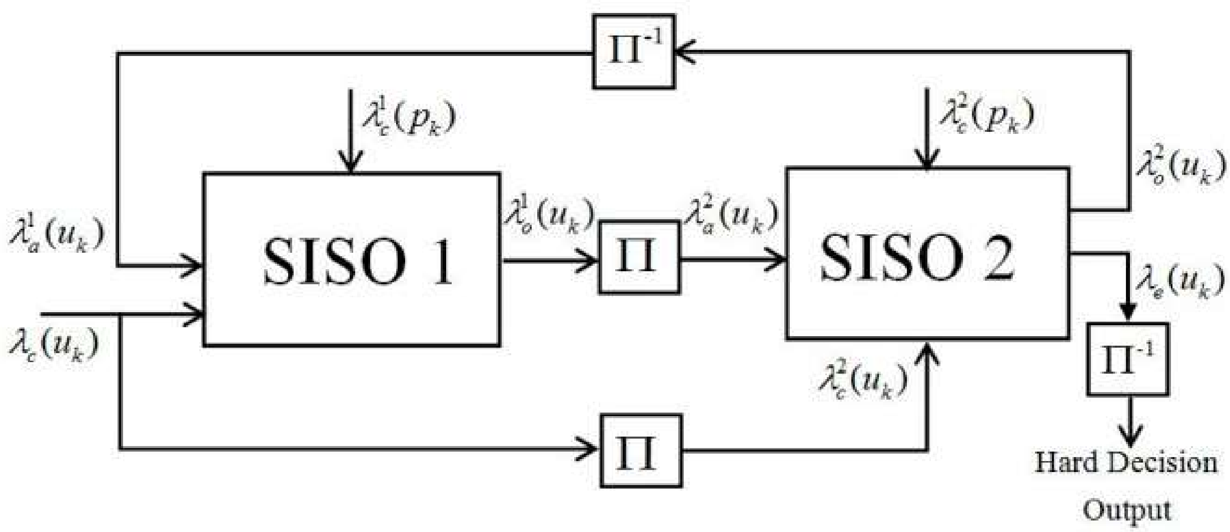
As shown in the example figure, decoding occurs (and occurred) from the first soft decision decoder, "upper decoder," to the second, or last, soft decision decoder, "lower decoder." The upper decoder outputs lets say "upper decoder output" which is fed as back as an input to the lower decoder. The upper decoder outputs "upper decoder output." This "upper decoder output" is fed as input into the lower decoder. The lower decoder is the last soft decision decoder in a circular circuit propagating from the upper decoder to the lower decoder to the upper … to the lower …to the upper… to the lower, etc. This process was performed a predetermined number of times as defined by the software governing the turbo decoding process. For example, the default number of iterations in the example given below is 8 iterations:

> "Throughput Calculation
>
> The throughput can be calculated using the following formula:
>
> These calculations are for running the Turbo decoder for 8 iterations (I = 8)

> Early Termination Support
>
> The CRC checksum generated by the SISO decoder outputs (both lower and the upper decoders in Figure 3 on page 7) are checked after every iteration. Rather than continuing until the maximum number of iterations specified at the input ports, the Turbo decoding is terminated as soon as the CRC results with success."

(*See, e.g.,* Altera Corporation, "3GPP LTE Turbo Reference Design" (Jan. 2020), *available at* https://www.intel.com/content/dam/www/programmable/us/en/pdfs/literature/an/an505.pdf Page 11 ("A Turbo decoder consists of two single soft-in soft-out (SISO) decoders, which work iteratively.")).

32. Additionally, all known commercial implementations of 4G LTE turbo decoders are iterative and functionally equivalent to the figure below. The figure below illustrates an output from the last soft decision decoder is fed back as an input to the first soft decision decoder, then from the first to the second decoders, and propagate to the last decoder in a circular circuit (*e.g.*, the a posteriori output of SISO 2 is de-interleaved with the associated memory module and fed as a priori input of SISO 1, while the a posteriori output of SISO 1 is interleaved with the associated memory module and fed as a priori input of SISO 2).



(*See* Jun Li et al., "Turbo Decoder Design based on an LUT-Normalized Log-MAP Algorithm," Entropy (Basel) (Aug. 20, 2019), *available at* https://www.ncbi.nlm.nih.gov/pmc/articles/PMC7515343/). Iterative turbo decoder implementations require completing a certain number of iterations to complete decoding a frame with a satisfactory degree of confidence. Iterative decoding must therefore be performed a predetermined number of times according to a stopping rule; *see, e.g.,* A. Matache *et al.*, "Stopping Rules for Turbo Decoders," TMO Progress Report 42-142 (Aug. 15, 2000), *available at* https://ipnpr.jpl.nasa.gov/progress_report/42-142/142J.pdf).

33. Plaintiff has been damaged as a result of Defendant's infringing conduct (including Defendant's use of the Accused Instrumentalities). Defendant is thus liable to Plaintiff for damages in an amount that adequately compensates Plaintiff for such Defendant's infringement of the '742 Patent, *i.e.*, in an amount that by law cannot be less than would constitute a reasonable royalty for the use of the patented technology, together with interest and costs as fixed by this Court under 35 U.S.C. § 284.

34. On information and belief, Defendant has had at least constructive notice of the '742 patent by operation of law and, to the extent required (no marking is required for method claims), marking requirements have been complied with.

IV. JURY DEMAND

Plaintiff, under Rule 38 of the Federal Rules of Civil Procedure, requests a trial by jury of any issues so triable by right.

V. PRAYER FOR RELIEF

WHEREFORE, Plaintiff respectfully requests that the Court find in its favor and against Defendant, and that the Court grant Plaintiff the following relief:

a. Judgment that one or more claims of United States Patent No. 6,813,742 have been infringed, either literally and/or under the doctrine of equivalents, by Defendant;

b. Judgment that Defendant account for and pay to Plaintiff all damages to and costs incurred by Plaintiff because of Defendant's infringing activities and other conduct complained of herein;

c. That Plaintiff be granted pre-judgment and post-judgment interest on the damages caused by Defendant's infringing activities and other conduct complained of herein; and

d. That Plaintiff be granted such other and further relief as the Court may deem just and proper under the circumstances.

March 4, 2025

BEUSSE SANKS, PLLC

/s/ Terry M. Sanks
Terry M. Sanks
Beusse Sanks, PLLC
612 E. Colonial Drive, Suite 250,
Orlando, FL 32803
407-644-8888
tsanks@firstiniplaw.com
litigation@firstiniplaw.com

OF COUNSEL:

David R. Bennett
(Motion for *pro hac vice* to be filed)
Direction IP Law
P.O. Box 14184
Chicago, IL 60614-0184
(312) 291-1667
dbennett@directionip.com

Attorneys for Plaintiff Turbocode LLC